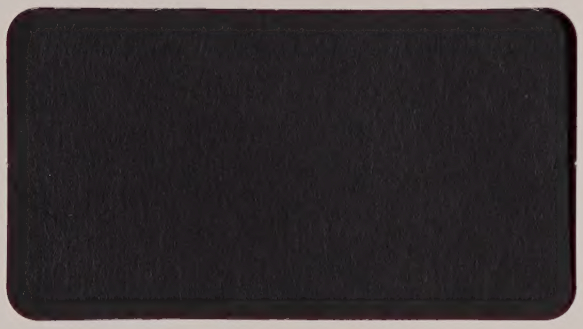

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 23-S-1184
12/32 MHz SYNTHESIZED FUNCTION GENERATOR

The Model 23-S-1184 is identical to the standard Model 23, as described herein, except that the standard instrument front panel is replaced with a 5-1/4 inch high rack mount front panel containing six feed-through BNC's.

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SAFETY FIRST

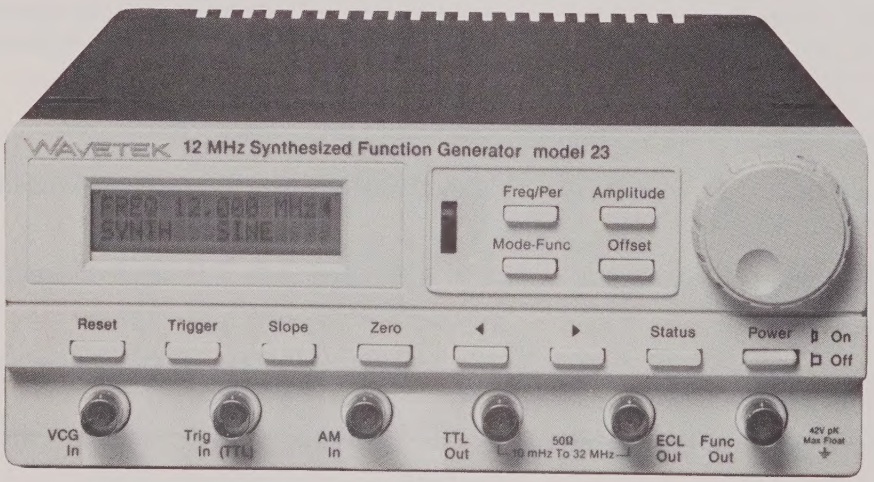
Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNING

This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.

Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potentially harmful lithium. Observe polarity when you replace the battery.


WAVETEK 12 MHz Synthesized Function Generator model 23
FREQ 12.000 MHz
SYNTH SINE
Freq/Per
Amplitude
Mode-Func
Offset
Reset
Trigger
Slope
Zero
Status
Power
On
Off
VCG In
Trig In (TTL)
AM In
TTL Out
50Ω 10 mHz To 32 MHz
ECL Out
Func Out
42V pk Max Float

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 23

The Wavetek 23 Function Generator generates a signal from 0.01 Hz to 12 MHz in synthesized, continuous, triggered and gated modes with output levels of 10 mV to 20 volts peak-to-peak. The synthesized mode has 4 digits of frequency resolution with 0.005% (50 ppm) accuracy. In addition, the synthesizer circuit extends ECL and TTL output frequencies to 32 MHz.

The Model 23 conventionally generates sine, triangle, and square waveforms from 12 MHz down to 1 kHz. Below 1 kHz the waveforms are digitally synthesized to extend the frequency range down to 0.01 Hz while at the same time maintaining high speed locking in the frequency synthesized mode. The waveform synthesizer also provides the additional features of up and down ramps, and triggered or gated haverwaves. A dc offset voltage is available up to ±10V peak.

Instrument set-up parameters are programmable and are displayed on a 16 character by 2 line LCD display. The Model 23's microprocessor makes possible the interactive display, remote programming, frequency and amplitude units conversion, and internal test procedure. The ability to power up in the same set-up as when last powered down is provided by a stored memory setting maintained with a long-life lithium battery.

The Model 23 also has the capability of being externally modulated using amplitude (AM), frequency (FM), or suppressed carrier (SCM) modulation. Carrier suppression is at least 40 dB, and may be improved to typically 70 dB (to 1 MHz) by using the Control knob to adjust the SCM NULL value.

GPIB (Option 001) numeric input is entered in free format (fixed, floating, or exponential notation). The parameters may be entered in any order and interactive error checks occur after the execute command. RS-232-C (Option 002) data format is 8-bit, no parity one stop bit.

Manual control parameters are key selected via the front panel. Numeric values are incremented or decremented with the prominent control knob with immediate error checking and execution.

Instrument setup is continuously battery backed-up in memory for return to exact setup after power-down. Memory is maintained with a non-rechargeable lithium battery for 6 months minimum (typically several years). A low battery warning will be displayed at power-up if the battery voltage drops to 70% of its nominal voltage.

WARNING

This equipment uses a BR-2/3A, 3V lithium battery, that contains less than 0.5 grams of lithium. To prevent the release of a potentially harmful substance, DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE BATTERY. In addition, observe correct polarity when replacing.

1.2 SPECIFICATIONS

1.2.1 Waveforms

Programmable sine, triangle, square, and dc are available from 1 kHz to 12 MHz. Below 1 kHz, up ramps and down ramps, and triggered or gated haversine or havertriangle waves. Above 12 MHz, only TTL and ECL clock waveforms are available.

1.2.2 Operational Modes

Continuous
Function, TTL, and ECL outputs are all active. Output is continuous at programmed frequency, 3 digit resolution and ±1% of programmed frequency.

Trigger
As in Continuous Mode except that output quiescent until triggered by external signal, interface (option 001) trigger, or manual trigger, then generates one cycle at programmed frequency.

Gate
Same as Triggered Mode except output is continuous for the duration of the gate signal. The last cycle started is completed.

Clock
Function output is 0 Vdc. TTL and ECL outputs are active to 32 MHz. Frequency is synthesized to 0.005% accuracy.

Continuous Synthesized
Same as Continuous Mode except 4 digit frequency resolution and 0.005% (50 ppm) accuracy.

1.2.3 Output Frequency

Range
10 mHz to 12 MHz in 9 decade ranges continuously programmable at Func Out. 10 mHz to 32 MHz continuously programmable at TTL Out and ECL Out if in the clock mode. 100 μHz is lowest attainable frequency (See Frequency Zero, paragraph 1.2.5).

Resolution
4 digits in synthesized modes. 3 digits in all other modes. Additional ¼ digit for frequencies above 10 MHz. Between 16 and 32 MHz the frequency steps are in two least significant digits (LSD).

Accuracy
50 ppm in synthesized and clock modes. ± 1% of frequency setting ± 1% of decade range in all other modes.

Spurious Signals
Typically 70 dB below fundamental (excluding fundamental ± 200 Hz) to 1 MHz and 40 dB below fundamental to 12 MHz (in synthesizer mode only).

Integrated Signal To Phase Noise
Typically 40 dB below the signal to 1 MHz measured over ± 15 kHz bandwidth excluding carrier ± 10 Hz (in synthesizer mode only).

Synthesized Mode Lock Time
Less than 300 ms for within 0.01% of new programmed frequency.

Repeatability (24 hr.)
0.0003% in synthesized mode. ± 1% in all other modes.

Jitter
Less than or equal to 0.1% of period, ± 100 picoseconds.

1.2.4 Frequency Control

Controlled by programmed value or by external VCG input.

Value
Frequency value is manually or bus programmable with automatic range selection.

VCG (Voltage Controlled Generator)
An ac or dc input voltage controls the frequency. This input is disabled in the synthesized mode. 0.0 to ± 12 volts into 10kΩ for up to 1200:1 frequency change in each of 9 frequency ranges (ranges must be programmed). Slew rate is limited to 0.1 V/μs.

1.2.5. Frequency Zero

In the non-synthesized modes, the front panel controls or the bus commands will set the frequency to the bottom of the current range for 1000:1 VCG change (1200:1 on top range only). The ranges are as follows:

Specified Range† (Programmable Portion)	Lowest Obtainable VCG or Zero Frequency
12.00 MHz to 1.00 MHz	10 kHz
999 kHz to 100 kHz	1 kHz
99.9 kHz to 10.0 kHz	100 Hz
9.99 kHz to 1.00 kHz	10 Hz
999 Hz to 100 Hz	1 Hz
99.9 Hz to 10.0 Hz	100 mHz
9.99 Hz to 1.00 Hz	10 mHz
999 mHz to 100 mHz	1 mHz
99.9 mHz to 10.0 mHz	100 μHz

*Waveform specifications are applicable.

1.2.6 Output Signals

Amplitude
Range: 0.01 to 10.2 Vp-p into selected impedance (0.02 to 20.4 Vp-p into ≥50kΩ) at Func Out. Impedance is user or option selectable to be 50, 75, or 600Ω*. Absolute peak amplitude plus offset may not exceed 5.1 volts into selected impedance (10.2 into ≥50 kΩ). Selected value may also be displayed in Vp, Vrms or in dBm.
Resolution: 3 digits or 10 mV when absolute peak amplitude plus offset >0.5V; 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V; 3 digits or 0.1 mV when absolute peak amplitude plus offset ≤0.05V. When in dBm units, actual resolution is the same. The closest decimal value to the dBm value asked for (in 0.1 dBm increments) will be given.
Accuracy: ± 1% of selected value plus one of the following; For 0.01 to 0.099 Vp-p (peak amplitude plus offset <0.05V) range, add ± 1 mV. For 0.1 to 0.999 Vp-p (peak

amplitude plus offset <0.5V) range, add ±10 mV. For 1.00 to 10.2 Vp-p range add ±100 mV.
Repeatability (24 hr.): ±1% of setting, ±10 mV.
Flatness (50)*: With reference to 1 kHz at 5 Vp-p; 0.2 dB to 100 kHz, 1.5 dB to 12 MHz.

DC Offset

Range: DC or offset programmable from −5.1V to +5.1V into selected impedance (−10.2V to +10.2V ≥50kΩ). Absolute peak amplitude plus offset may not exceed 5.1V into selected impedance (10.2V into ≥50kΩ).
Resolution: 3 digits or 10 mV when absolute peak amplitude plus offset ≥0.5V, 3 digits or 1 mV when absolute peak amplitude plus offset <0.5V, 3 digits or 0.1 mV when absolute peak amplitude plus offset <0.05V.
Accuracy: dc function; ±1 mV for <50 mV; ±6 mV for ≥50 mV to <0.50V; ±60 mV for ≥0.50V.
Repeatability: ±1% of setting ±20 mV.

1.2.7 Output Characteristics

Func Out
Source of primary waveforms. Peak output current is 100 mA maximum with a standard source impedance of 50Ω. Output is protected against a short circuit to any voltage between ±10 Vdc. Includes internal fused protection in the output conductor against accidental application of up to 250 Vac or 350 Vdc. Source impedance is selectable as 50, 75 or 600Ω.

TTL Out

Output conductor is fuse protected against accidental output short circuits. Source impedance is 50Ω.

ECL Out

Source impedance is 50Ω into −2V. Output is protected against short circuits into +1 to −5.2 Vdc.

1.2.8 External Inputs

VCG In (10KΩ)
For external voltage control of generator frequency. (See Frequency Control). Except in the synthesizer mode, the VCG voltage, as well as programming, selects the generator frequency. Frequency may be programmed or ac-modulated (FM and sweep) by external 0 to +12V signal. VCG input can change generator frequency 1200:1 over each range, upper and lower frequencies limited to maximum and minimum of selected range (with 20% overrange on upper limit).

Signal bandwidth: 100 kHz maximum.
Slew rate: 0.1 V/μs maximum.
Input impedance: 10kΩ.

Trig In (TTL)

For external TTL compatible input signals to trigger or gate the generator on in triggered and gated modes. Positive or negative edge triggering or high or low level gating is programmable.

Signal pulse width: 50 nanoseconds minimum.
Repetition rate: 5 MHz maximum.

AM In (600Ω)

Input for external ac signal to provide amplitude modulation (AM) or suppressed carrier modulation (SCM) envelope. The function generator waveform instantaneous amplitude is a function of modulating signal. Peak amplitude plus offset at Func Out is still limited to ±10.2V open circuit (±5.1V into selected impedance). Amplitude Zero selection causes the carrier dc amplitude to be zero volts to provide SCM via the AM In (600Ω) connector. Carrier suppression is initially at least 40 dB (including carrier, modulator and both squared terms) and may be further improved to typically 70 dB carrier null at low frequencies using SCM NULL and Control knob.

Scale factor: 1 V/V (≥0.5 Vp amplitude) [i.e., ±5V AM input will amplitude modulate a 5V carrier 100% (from 10V to 0V)]. Selectable to 0.1 V/V or 0.01 V/V by programmed amplitude.
Input impedance: 600Ω.

1.2.9 Waveform Characteristics

Func Out

Sine Distortion (THD at 10 Vp-p): Less than 0.5% from 0.01 to 9.99 kHz; less than 1.0% from 10.0 kHz to 99.9 kHz.
No harmonics above: −40 dBc from 100 kHz to 999 kHz; −27 dBc from 1 MHz to 12 MHz (50Ω)*.
Time Symmetry: ±1% of setting, ±8 ns. ±0.1% <1 kHz.
Square Transition Time: <25 ns (50Ω)*.
Square Peak-to-Peak Aberrations: Less than 5% at full amplitude (50Ω)*.
Triangle Linearity: 99% up to 100 kHz.

TTL Out

TTL compatible pulse with 50% duty cycle at programmed frequency. Level is ≤0.4 to ≥2.0V into 50Ω, ≤0.4 to ≥4.0V into ≥50kΩ. Timing is concurrent with square function output and lags sine and triangle by 90° in all modes and up to 12 MHz. Above 12 MHz (in clock mode), the Function Output is quiescent and TTL output is at programmed frequency up to 32 MHz. TTL waveform has <10% peak aberrations into 50Ω.

ECL Out

Same characteristics as the TTL output, except that levels are ECL compatible when loaded by 50Ω into −2V. Waveform has <5% peak aberrations into 50Ω.

1.2.10 LCD Display

2 lines of up to 16 alphanumeric characters. Viewing angle is adjustable.

1.2.11 General

Stability

Amplitude, frequency (non-synthesized) and dc offset: After 30 minutes warm-up; ±0.1% of range for 10 minutes and ±0.5% of range for 24 hours.
Frequency (Synthesized): ±1 ppm/°C between 0°C and +50°C. Crystal is 6.144 mHz with 0.005% accuracy and aging rate of 20 ppm/year.

Environmental

Temperature: Specifications apply at 23°C ±5°C. Operates 0°C to +50°C. −20°C to +75°C for storage.
Vibration: 5 to 55 Hz with maximum of 2g at 55 Hz.
Shock: 30g, 11 ms half sine.
Altitude: Sea level to 10,000 ft. for operation. Sea level to 40,000 ft. for storage.
Relative Humidity: 95% at up to 60°C for storage, 45% at up to 50°C and 75% at up to 25°C at sea level (non-condensing) for operation.

Dimensions
211 mm (8.3 in.) wide, 85 mm (3.4 in.) high, 305 mm (12 in.) deep.

Weight
4.0 kg (8.8 lb) net, 5.0 kg (11 lb) shipping.

Power
90 to 110, 105 to 125, 180 to 220, 210 to 250V selectable, 48 to 66 Hz, less than 50 VA.

Options

001: GPIB Programming**
IEEE 488-1978 compatible, Non-isolated, Double buffered.
Address: 0-30 internal switch selectable.
Subsets: SH1, AH1, T6, TE0, L4, SR1, RL1, PP0, DC1, C0, E1.

002: RS-232C Serial Port:**
Rear panel mounted DB-25 conector.
Connector: DB-25 (female) with DCE or DTE configuration.
Mode: Full Duplex (bi-directional) with CTS/DTR or XON/XOFF handshaking.
Data Format: 8 bits, no parity, one stop bit.
Data Rate: 14 step selectable (50, 75, 110, 134.5 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200).

003: 75Ω Function Output Impedance

004: 600Ω Function Output Impedance

---

* Applicable when source and load impedances are 50Ω respectively. Higher source impedances (Options 003 and 004) will have derated high frequency characteristics. High frequency characteristics are also subject to variations due to output cable lengths.

** "Factory installed" options only.

All specifications apply for programmed amplitude of 10 Vp-p into 50Ω.

SECTION 2
INITIAL PREPARATION

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Line Voltage

Refer to table 2-1 to determine the proper selection of the line voltage connector. Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 1/2 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit and a ¼ amp fuse installed.

2.2.2 Verifying the Line Voltage

To verify the line voltage (or change the fuse), the operator must first remove the top and bottom covers. Remove the top and bottom covers using the following steps and figure 2-1.

CAUTION

All calibration pots are located inside the bottom cover on the circuit board. Be careful not to change the setting of any potentiometers, as this may require a recalibration of the instrument.

1. Remove two (2) screws holding top and bottom covers to rear panel.
2. Slide both covers (together as a unit) to the rear and remove from the chassis assembly.

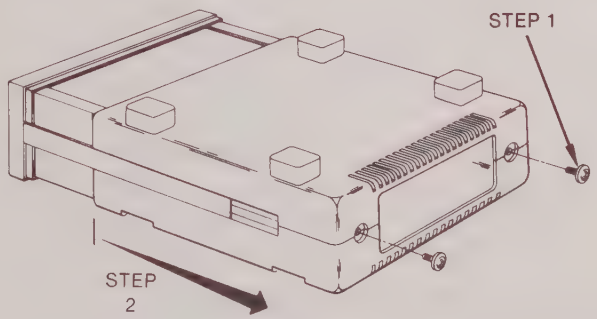


Figure 2-1. Top and Bottom Cover Removal

After the covers have been removed, the line voltage can be checked by viewing the voltage label through the inspection hole as shown in figure 2-2.

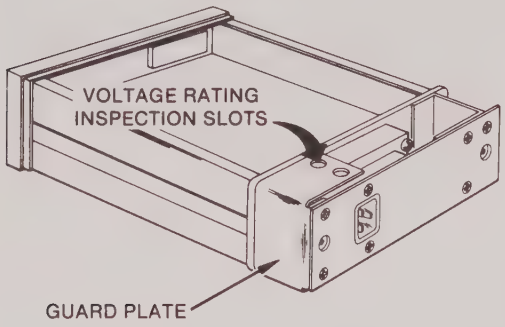


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct according to table 2-1, perform the following steps and refer to figure 2-3 for step 1, and figure 2-4 for steps 2 thru 4 to change the line voltage and fuse.

1. Remove two screws holding guard plate to the rear panel.

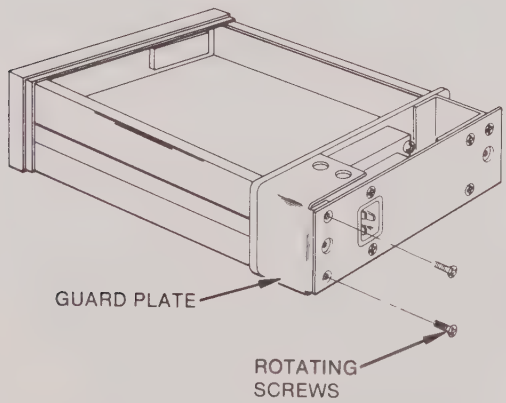


Figure 2-3. Guard Plate Removal

2. Remove the voltage selector connectors from the ac primary board. Rotate the connector or connectors until the correct voltage selector indicator is on top.
3. Reinstall the voltage selector connectors.
4. Remove the fuse and install new fuse as called out in table 2-1.

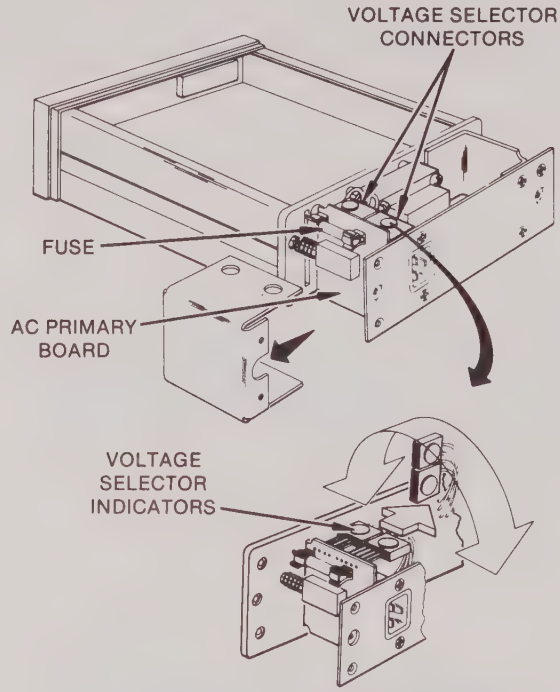


Figure 2-4. Fuse and Voltage Selection

Table 2-1. Voltage/Fuse Selection

Connector Position	Voltage Range	Fuse
115V LO	90 to 110 Vac	1/2 amp Slo-Blo
115V HI	105 to 125 Vac	1/2 amp Slo-Blo
220V LO	180 to 220 Vac	1/4 amp Slo-Blo
220V HI	210 to 250 Vac	1/4 amp Slo-Blo

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the guard plate is attached to the unit.

Reassembly

Refer to figure 2-5 for steps 1 thru 3 and figure 2-6 for steps 4 thru 6.

1. Align the guard plate and check the routing of all wires to prevent pinching wires between the transformer and guard plate.
2. Verify that the power rod extends through the front panel slot, the circuit board seats correctly in the

power supply panel slot, and the wires are routed correctly.

3. Align the guard plate with the rear panel and then secure with two screws.

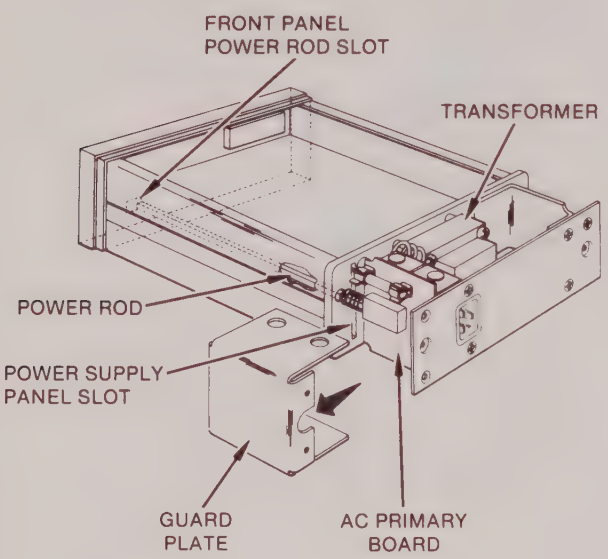


Figure 2-5. Rear Chassis Assembly

4. Turn the instrument upside down, position the bottom cover over the guard shield, and then slide the bottom cover forward approximately two (2) inches while engaging the top cover shield slides (see figure 2-6, detail A) and the outside slide rails (see figure 2-6, detail B).
5. Turn the instrument right side up. Install the top cover using the same procedure as in step 4.
6. Align the rear of both the top and bottom cover with each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly together and slide the chassis assembly into top and bottom covers.

CAUTION

When sliding on the bottom cover, avoid pinching any coaxial cables located near the front panel.

7. Secure covers to unit using two screws as shown in figure 2-1.

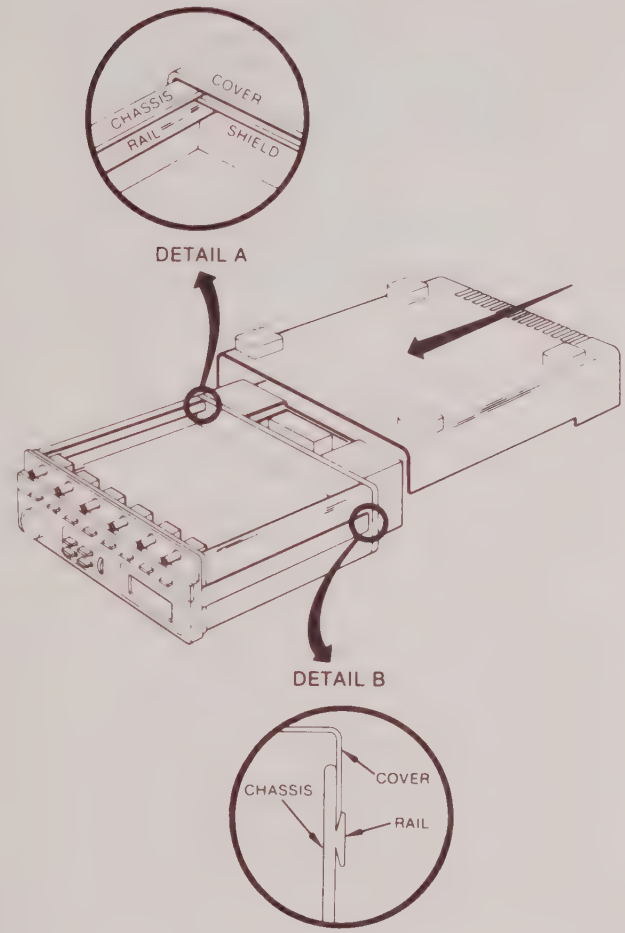


Figure 2-6. Top and Bottom Cover Installation

2.2.4 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

NOTE

Signal ground may be floated up to ±42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.2.5 GPIB Interface Connections

The GPIB (Option 001) I/O rear panel pin connections and signal names are given in table 2-2. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

NOTE

The terms "GPIB" and "IEEE-488" are used interchangably in this manual.

Table 2-2. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Chassis Ground	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

2.2.6 GPIB Address

For OPT 001 instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB address can be changed by the internal switch (figure 2-7) or the front panel STATUS key (rotate knob when GPIB ADRS is displayed). (See figure 2-1 for cover removal, 2-6 for installation.)

The switch sections are labeled from 1 through 5 and their OPEN position noted (OPEN = Binary "0" in table 2-3). To verify the address, press STATUS on the front panel. The device number (decimal) will be displayed. Upon power-up, the address is always that of the internal switch.

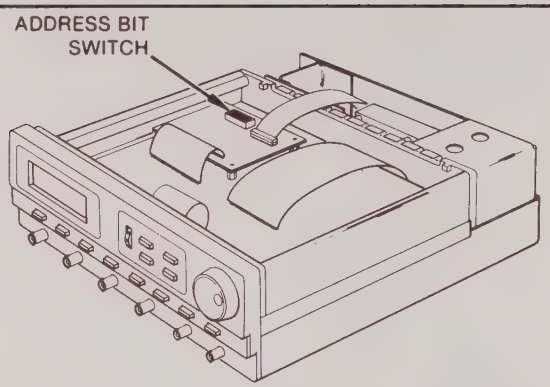


Figure 2-7. GPIB Address Bit Switch

Table 2-3. GPIB Address Codes

Device	ASCII Listen	ASCII Talk	Switch Position 1 2 3 4 5	Hexa-decimal Listen	Hexa-decimal Talk
0	(space)	@	0 0 0 0 0	20	40
1	!	A	1 0 0 0 0	21	41
2	"	B	0 1 0 0 0	22	42
3	#	C	1 1 0 0 0	23	43
4	$	D	0 0 1 0 0	24	44
5	%	E	1 0 1 0 0	25	45
6	&	F	0 1 1 0 0	26	46
7	'	G	1 1 0 0 0	27	47
8	(	H	0 0 0 1 0	28	48
9	)	I	1 0 0 1 0	29	49
10	*	J	0 1 0 1 0	2A	4A
11	+	K	1 1 0 1 0	2B	4B
12	,	L	0 0 1 1 0	2C	4C
13	—	M	1 0 1 1 0	2D	4D
14	.	N	0 1 1 1 0	2E	4E
15	/	O	1 1 1 1 0	2F	4F
16	0	P	0 0 0 0 1	30	50
17	1	Q	1 0 0 0 1	31	51
18	2	R	0 1 0 0 1	32	52
19	3	S	1 1 0 0 1	33	53
20	4	T	0 0 1 0 1	34	54
21	5	U	1 0 1 0 1	35	55
22	6	V	0 1 1 0 1	36	56
23	7	W	1 1 1 0 1	37	57
24	8	X	0 0 0 1 1	38	58
25	9	Y	1 0 0 1 1	39	59
26	:	Z	0 1 0 1 1	3A	5A
27	;	[	1 1 0 1 1	3B	5B
28	<	\	0 0 1 1 1	3C	5C
29	=	]	1 0 1 1 1	3D	5D
30	>		0 1 1 1 1	3E	5E

NOTE Address 31 is not allowed.

2.2.7 The RS-232 Connector

The RS-232-C I/O rear panel pin connections and signal names are given in table 2-4. The panel connector is a DB-25 female connector (see figure 2-8) and will connect to a standard RS-232-C cable (interface type E). The data format is an 8-bit, no parity, one stop bit.

Table 2-4. RS-232 Data In/Out

Pin	Name	Direction (DCE Configuration)	Direction (DTE Configuration)
2	TXD[1]	IN	OUT
3	RXD[2]	OUT	IN
4	RTS[3]	N/C	OUT
5	CTS[4]	OUT	IN
6	DSR[5]	OUT	IN
7	SIG GRD	—	—
8	RLSD[6]	OUT	IN
20	DTR	IN	OUT

(Remaining Pins Not Connected)

[1]Transmit Data
[2]Receive Data
[3]Request to Send
[4]Clear to Send
[5]Data Set Ready
[6]Receive Line Signal Detect

The baud rate is selectable from those listed in table 2-5 using dip switch SW1 (figure 2-9).

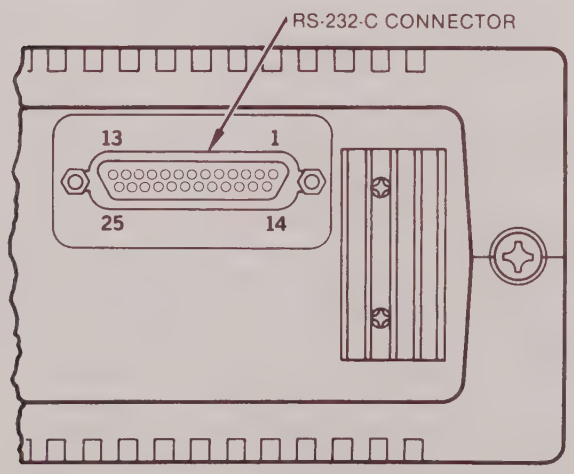


Figure 2-8. RS-232-C Connector Pinouts

2.2.8 Connecting the RS-232-C Interface

Before connecting the Model 23 RS-232-C interface, the correct configuration (DCE or DTE) must be selected and the internal ribbon cable connected to either the DCE or DTE location (figure 2-9) on the RS-232-C option board.

To determine which configuration is correct obtain the manual for the system controller/computer. This device must have a DB-25 RS-232-C connector.

1. Determine if the controller is a DCE device or a DTE device. If this is not explicitly spelled out you will need to look at the pin out for its connector. If pin 2 is the data output, the device is a DTE (most computers). If pin 3 is the data output, the device is a DCE (most modems). Configure the Model 23 as the opposite type of device by connecting the internal option cable to the appropriate header (figure 2-9). (See figure 2-1 for cover removal, 2-6 for installation.)
2. In most cases a straight through cable can be used to connect the Model 23 with the other device. The Model 23 only requires the connection of pins 2, 3, 5, 7, and 20 but the other device may require more. Examples of typical cable assemblies are shown in figure 2-10. However, there are many interpretations of the RS-232-C standard and either of the following procedures (A or B) should be used to ensure that the control and handshake signals are properly connected.
   a. If the Model 23 is configured as a DCE then;
      (1) Pin 7 is always straight through.
      (2) Pins 2 and 3 are connected straight through if DCE/DTE configuration is correct.
      (3) Pin 5 of the Model 23 will need to be connected to an input of the other device that will enable and disable the character transmission from that device. If the other device does not support this, XON/XOFF handshaking will need to be used and pin 5 can be left disconnected.
      (4) Pin 20 of the Model 23 should be connected to an output pin on the other device that indicates when it is ready to accept data. If the other device does not have such a pin but is always ready, it can send XOFFs and XONs to indicate readiness. When using this method, or if the other device is always ready to accept data, this pin can be connected to an always positive pin on the other device or to pin 6 or 8 on the Model 23.
      (5) Pins 6 and 8 are always positive when the power is On. They can be connected to any pins on the other device that must be held positive.

b. If the Model 23 is configured as a DTE then;

(1) Pin 7 is always connected straight through.

(2) Pins 2 and 3 are connected straight through if DCE/DTE configuration is correct.

(3) Pin 20 of the Model 23 will need to be connected to an input of the other device that will enable and disable the character transmission from that device. If the other device does not support this, XON/XOFF handshaking will need to be used and this can be left disconnected.

(4) Pin 4 is always positive when the power is On and can be connected to any pin on the other device that must be held positive.

(5) Pins 6 and 8 are properly terminated inputs but have no function.

(6) Pin 5 tells the Model 23 that the connected device is ready to receive data. If the other device is always ready, pins 4 and 5 of the Model 23 may be connected together.

NOTE

Any pins not mentioned in the previous list are not connected in the Model 23 and therefore can be connected to anything if the connections are already present in the cable.

3. The handshaking method is front panel selectable as CTS/DTR (Clear to Send/Data Terminal Ready) (hardware) or XON/XOFF (Data Transfer On/Data Transfer Off.

4. Set the baud rate on the Model 23 to the highest rate that is available on both the Model 23 and the controller/computer. This is done by setting the dip switches (figure 2-9) according to table 2-5.

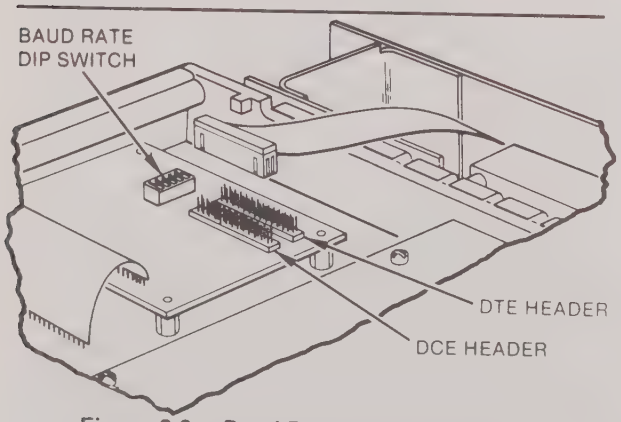


Figure 2-9. Baud Rate Dip Switch and DTE/DCE Connections

Table 2-5. RS-232-C Baud Rate Codes

Baud Rate	SW1- 4	3	2	1
*9,600	1	0	0	0
4,800	1	0	0	1
2,400	0	1	1	1
1,800	1	0	1	0
1,200	1	0	1	1
600	0	1	1	0
300	1	1	0	1
200	0	1	0	1
150	1	1	1	0
134.5	0	1	0	0
110	1	1	1	1
75	0	0	1	1
50	0	0	1	0

0 = Closed = On
1 = Open = Off
*This is the factory set position.

NOTE

1. SW1-5 should always be OPEN.

2. Factory connector configuration is DCE.

5. Configure the controller/computer for the same baud rate as in step 4, 1 stop bit, 8 data bits, and no parity.

2.3 INITIAL CHECKOUT PROCEDURE

The checkout procedure in table 2-8 is to be used only as a receiving inspection or post-repair checkout. The procedure verifies functional operation of this instrument but does not verify the calibration. The frequencies shown are typical values and should be used only as a guide. Required tools and test equipment are given in table 2-6.

The checkout procedure must be used starting with the first step and continuing through to the last step. Do not move or change any control or switch unless specifically instructed to do so by the procedure. If a step instructs you to press a switch until the annunciator points left or right, or to a specific display name, do so by pressing once, observing the display, and if required, pressing it again until the proper indication is obtained. Remember, each step in the procedure is dependent on the preceeding step for the correct position of all controls and switches. (Refer to section 3 for descriptions of the controls.)

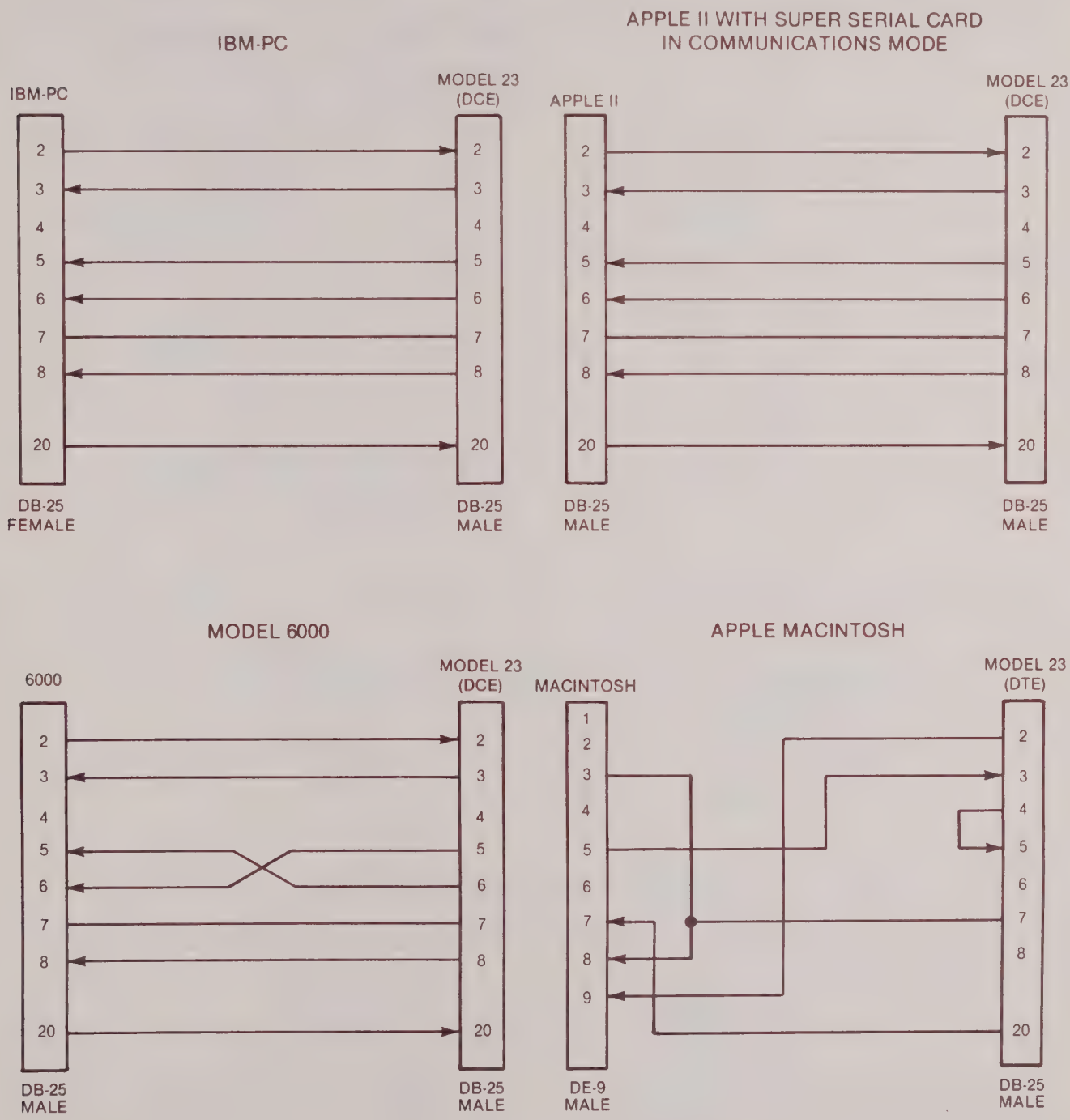


Figure 2-10. Typical Examples of Serial Cables

Prior to starting the checkout procedure, connect an oscilloscope and frequency counter to the Model 23 as shown in figure 2-11. Set the test equipment controls as indicated in table 2-7.

Table 2-6. Test Equipment and Tools

Instrument	Comments
Oscilloscope	Bandwidth: 100 MHz
Freq Counter	Frequency: > 50 MHz Sensitivity: >30 mV
50Ω Feedthrough	Accuracy: 0.5% Power: 2W
BNC Tee	1 Male, 2 Female connectors
BNC Coax Cable	RG58U, 3 ft. length (2 ea)

Table 2-7. Test Equipment Setup

Step	Equipment	Position/Operation
1	Oscilloscope	Power Switch: ON Vert Input: CH1 or 2 Vert Position: Center Trace Vert Coupling: DC Vert Sensitivity: .5 V/DIV Horiz Position: Center Trace Horiz Sweep: .2 ms/DIV Trig Level: (+) Positive Trig Polarity: (+) Positive Trig Mode: Auto Trig Coupling: AC Trig Source: Internal X10 Mag: Out (Off) Other Controls: As required
2	Freq. Counter	Mode: Frequency Trigger Level: As required

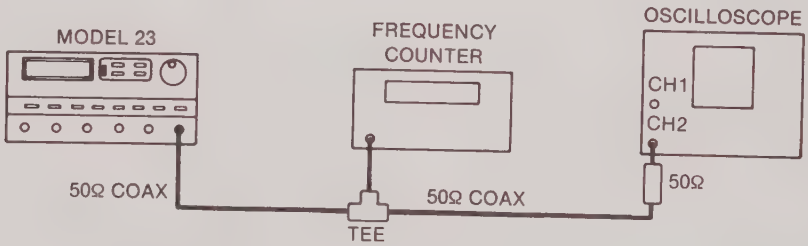


Figure 2-11. Equipment Checkout Interconnection

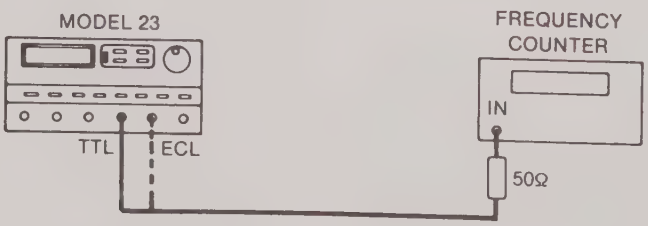


Figure 2-12. Check Frequency Output Setup

Table 2-8. Checkout Procedure

Step	Control/Switch	Position/Operation	Observation
1	Power	On (Position vertical thumb-wheel for best display.)	Display will indicate settings that were stored in memory.
2	Reset	Press Once	Display indicates: FREQ 10.00 KHZ ◄ CONT SINE
3	Control knob	Rotate CCW until the display reads 999 Hz.	
4	Mode-Func	Press once or twice to have annunciator arrow (<) point to the "Mode" section of the display.	
5	◄ switch	Press one or more times until SYNTH appears in the "Mode" section of the display.	
6	Amplitude	Press one time	Display annunciator (◄) will point to the "Amplitude" section of the display.
7	Control knob	Rotate CCW until display reads 1.00 Vp-p.	Verify that the oscilloscope displays approximately 2 cycles of a sine wave with an amplitude of 1 Vp-p.
8	Mode-Func	Press two times	Display annunciator (◄) will point to the "Waveform" section of the display.
9	► switch	Press one time	Verify that the display reads "SQUARE", the oscilloscope displays a square wave, and the frequency counter reads below 1 kHz.
10	► switch	Press one time	Verify that the display reads "TRIANGLE", the oscilloscope displays a triangle wave, and the frequency counter reads below 1 kHz.
11	► switch	Press one time	Verify that the display reads "RMP UP", the oscilloscope displays a positive-going ramp waveform, and the frequency counter reads below 1 kHz.

Table 2-8. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation
12	► switch	Press one time	Verify that the display reads "RMP DN", the oscilloscope displays a negative-going ramp waveform, and the frequency counter reads below 1 kHz.
13	► switch	Press one time	Verify that the display reads "DC", the oscilloscope displays a 0.0 Vdc baseline, and the frequency counter reads all zeroes.
14	Offset	Press one time	
15	Control knob	Rotate CW until display reads 1.00V.	Verify that the oscilloscope baseline is approximately +1V.
16		Rotate CCW until display reads −1.00V.	Verify that the oscilloscope baseline is approximately −1V.
17	Zero	Press one time	Display and oscilloscope show zero volts offset.
18	Mode-Func	Press one time	Display annunciator (◄) will point to the "Waveform" section of the display.
19	► switch	Press one time	Verify that SINE appears in the "Waveform" section of the display.
20	Mode-Func	Press one time	Verify that the annunciator (◄) points to the "Mode" section of the display and the word SYNTH appears.
21	► switch	Press three times	Verify that the annunciator (◄) points to the "Mode" section of the display and the word GATED appears.
22	Trigger	Press and hold.	Verify that the oscilloscope displays a sine waveform only during the time that the Trigger switch is pressed and held in.
23	◄ switch	Press one time	Verify that the annunciator (◄) points to the "Mode" section of the display and the word TRIG appears.

Set oscilloscope TRIG MODE to NORM and increase the intensity as required.

Table 2-8. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation
24	Trigger	Press as required	Oscilloscope will display a single cycle of sine wave each time the Trigger switch is pressed.
Disconnect oscilloscope cable from Func Out connector. Connect frequency counter to the TTL Out connector as shown in figure 2-12.			
25	◄ switch	Press three times	Verify that the annunciator (◄) points to the "Mode" section of the display and the word CLOCK appears.
26	Freq/Per	Press one time	
27	Control knob	Rotate CW until the display reads 32 MHz.	Verify that the frequency counter reads approximately 32 MHz.
Disconnect the frequency counter cable from the TTL Out connector and connect to the ECL Out connector.			
28			Verify that the frequency counter reads approximately 32 MHz.

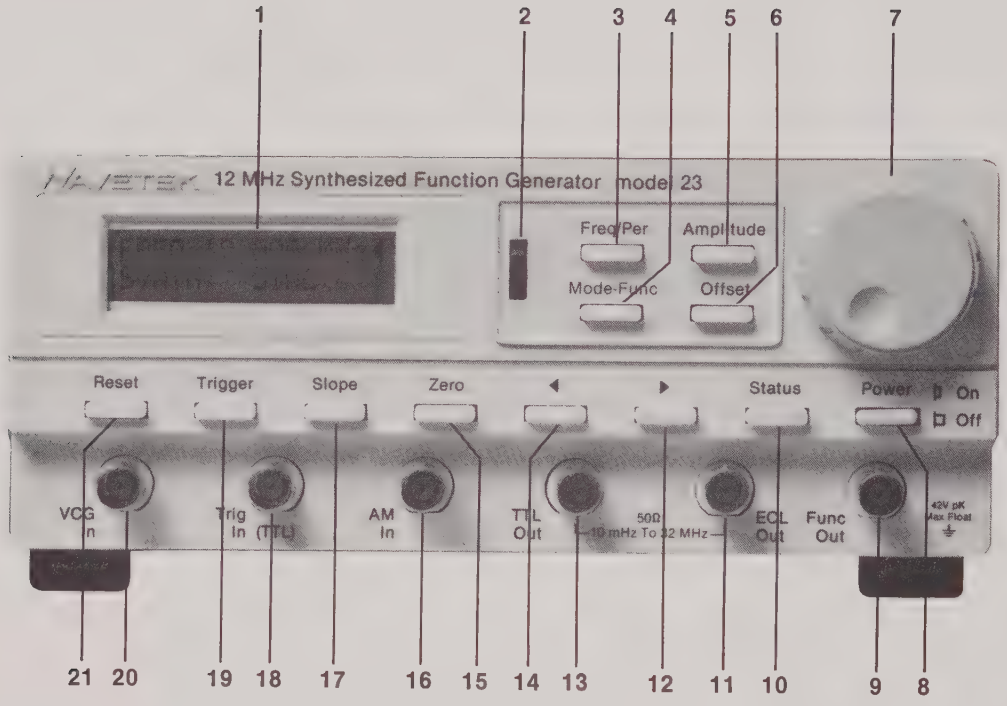


Figure 3-1. Controls, Connectors, and Indicators

SECTION 3
OPERATION

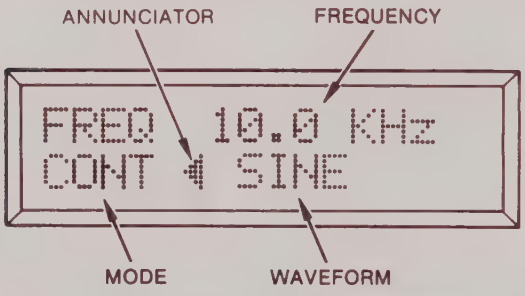
3.1 INTRODUCTION

This section describes the operation of the Model 23. The first part describes the controls and connectors; the remaining part describes how to use the various functions, modes and remote options.

3.2 CONTROLS AND CONNECTORS

The front panel controls and connectors are shown in figure 3-1 and keyed (bold numbers) to the following descriptions.

1 **Display** (See figure 3-2). This display will read out simultaneously up to three generator display functions depending on which switches have been pressed. An annunciator arrow appears to the right of the selected display function to indicate the function under immediate control. Moving the annunciator arrow allows other display functions to be selected and controlled.



FREQUENCY, MODE, AND WAVEFORM DISPLAY (MODE SELECTED)

AMPLITUDE AND OFFSET VOLTAGE DISPLAY (AMPLITUDE VOLTAGE SELECTED)

Figure 3-2. Display Indications

2 **Viewing Control.** This control allows the user to adjust the viewing angle of the LCD to optimize display legibility.

3 **Freq/Per Switch.** This switch will cause the display to show the generator output either in frequency or in time period. If frequency display is selected, then pressing the Freq/Per switch a second time will cause the display to show the output as a time period. Generator output frequency/period can only be changed if the annunciator arrow is pointing to the frequency or time period.

4 **Mode-Func Switch.** Pressing this switch causes the annunciator arrow to select either the generator mode or the output waveform. If the generator mode was displayed first (annunciator pointing to the left), pressing the switch a second time will select the output waveform. The opposite is also true if the output waveform was displayed first (annunciator pointing to the right). The generator mode or output waveform can only be changed while it is selected.

5 **Amplitude Switch.** When the amplitude switch is pressed, it selects the amplitude function of the display. Pressing the amplitude switch one, two, or three more times allows the amplitude to be displayed in Vpp, Vp, Vrms, or in dBm. The generator output amplitude can be changed only while the annunciator arrow is pointing to the display amplitude function.

6 **Offset Switch.** This switch selects the offset voltage function and displays it on the LCD display. The offset voltage can be changed only while the annunciator arrow is pointing to the display offset function. When the zero switch is pressed (after OFST is selected) the offset is zeroed out (0.00V).

7 **Control Knob** Allows the user to manually change any of the values or conditions of the selected display function. The frequency, period, amplitude, mode, function, offset voltage, and trigger slope can all be changed by rotating the control knob.

8 **Power Switch.** This switch turns the instrument On or Off. At power-up the instrument initializes to the conditions existing when the instrument was last powered-down.

9 **Func Out Connector.** This BNC connector is the main output for sine, square, triangle, up ramps, down ramps, and dc waveform. The output frequency range of this connector is 10 mHz to 12 MHz (down to 100 μHz in external VCG control). The maximum voltage output amplitude is 10 Vp-p into a 50Ω load (20 Vp-p into open circuit). Standard source impedance is 50Ω with 75Ω and 600Ω as options. This connector is not functional above 12 MHz and is internally fuse protected against accidental application to high voltage.

10 **Status Switch.** Allows one switch operation to check frequency, period, mode, function, amplitude, offset, trigger slope, battery condition, interface option if installed and its version. Each time the status switch is pressed a different display is presented until all have been monitored.

11 **ECL Out Connector.** This output (0.1 mHz to 32 MHz) is an ECL square wave at the frequency of the generator. No other waveforms are available from this connector. The display annunciator arrow must indicate CLOCK mode for frequencies above 12 MHz. This output is protected against short circuits into +1 to −5.2 volts.

12 **Right Arrow Switch (►).**

Display Annunciator Pointing To:	► Switch Steps Through:
Any mode	Each mode
Any waveform	Each waveform
Any frequency	Each decade range
Any amplitude	Each decivolt range
Any offset	Each decivolt range
Any frequency in VCG operation	Each decade range of frequency and each decade range of VCG rate
Any SCM null	Each decade range of AM rate

NOTE

With Option 001 or 002 installed, refer to paragraph 3.4.3.

13 **TTL Out Connector.** The output (0.1 mHz to 32 MHz) from this connector is a TTL square wave at the frequency of the generator. No other waveforms are available from this connector. The display annunciator arrow must indicate CLOCK mode for frequencies above 12 MHz. The output is internally fuse protected against external short circuits.

14 **Left Arrow Switch (◄).** This switch performs the same operations as the right arrow switch except that the display changes are performed in the reverse order.

15 **Zero Switch.** The zero switch performs the following functions:

- If frequency or period are selected, sets the instrument for VCG operation by setting the zero-FM frequency, the input sensitivity for the VCG input connector, and extending the bottom frequency by 2 decades.
- Zeroes the dc offset voltage if offset is selected.
- If amplitude is selected, Suppressed Carrier Modulation (SCM) operation and sets the output amplitude to zero.

16 **AM In (600Ω) Connector.** This connector inputs an ac signal for amplitude modulation (AM) or for Suppressed Carrier Modulation (SCM). For AM operation, a ±5V input will modulate a carrier 100% (amplitude 5 Vp-p and ext AM 10 Vp-p). The AM scale factor depends on the output attenuator range. For SCM operation, the zero switch will set the carrier dc amplitude to zero volts.

17 **Slope Switch.** This switch alternates the selection of the positive-going or the negative-going portion of the trigger input waveform for generator triggering or gating.

18 **Trig In (TTL) Connector.** This connector accepts a programmable or negative TTL level input (t_1) to trigger or gate the generator output as shown in figure 3-3. When triggered, the generator produces one complete cycle for each trigger input. When gated, the generator produces continuous cycles until the gate signal (t_2) is removed. The last cycle started is always completed (t_3). The negative-going edge of the TTL input will end gated operation.

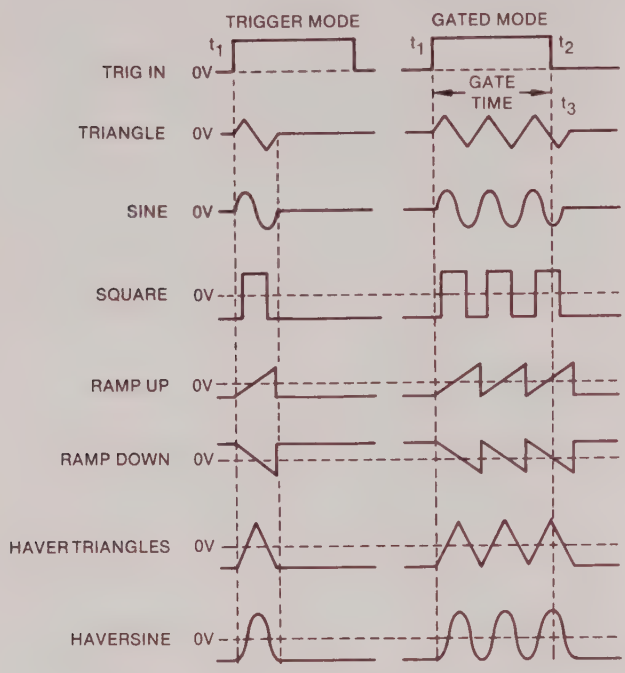


Figure 3-3. Output Waveforms

19 **Trigger Switch.** (See figure 3-3) In the triggered mode, pressing this switch manually initiates a single cycle of waveform each time it is pressed. In the gated mode, the trigger switch gates the output on until the switch is released. The last waveform cycle started while the switch is being pressed will be completed. If Option 001 or 002 is installed, see paragraph 3.4.2.

20 **VCG In (10KΩ) Connector** (See figure 3-4). This connector inputs an external voltage to control the generator frequency for sweep or FM operation. Operation is limited to the front panel selected or preprogrammed frequency range. Input control voltages are limited to positive voltages between 0 and + 10 Vdc (+ 12 Vdc on top range) or a 10 Vp-p maximum voltage centered at + 5Vdc (12 Vp-p centered at 6 Vdc for the top range). Positive-going voltage levels increase the frequency, while negative-going inputs decrease the frequency. Frequency excursions of 1000:1 (1200:1 on the top range) are possible in each of the frequency ranges. If the zero switch is pressed, the nine standard frequency ranges are down-shifted by 2 decades allowing a VCG bottom control range of 100 μHz. Input impedance is 10kΩ and maximum slew rate is 0.1V/μs.

21 **Reset Switch.** This switch resets all of the generator operating conditions to a preselected set of values as follows:

Frequency	10.0 kHz
Mode	Continuous
Waveform	Sine
Amplitude	5.00 Vp-p
Offset	0.00V
Slope	Positive

3.3 OPERATION

Perform the initial checkout procedure in Section 2 for a feel of the instrument. Information concerning individual controls and connectors may be found in paragraph 3.2. Output waveforms are shown in figure 3-3.

During the following set-up, the test equipment controls may have to be adjusted.

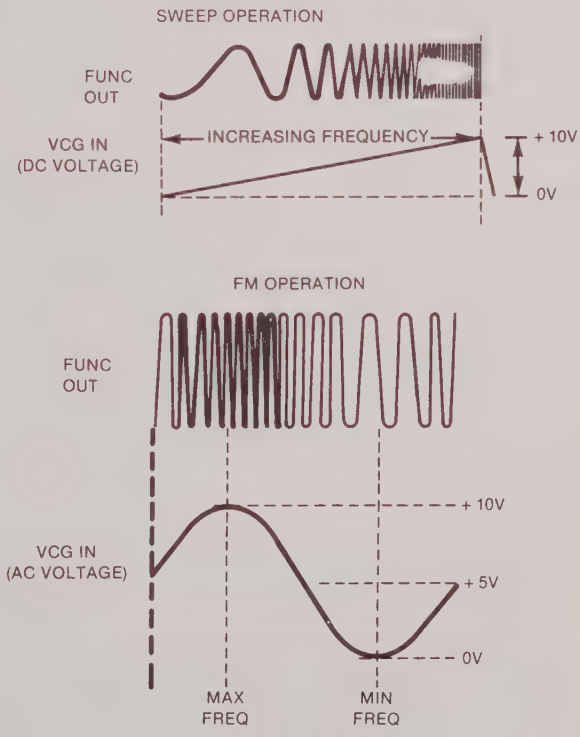


Figure 3-4. Sweep and FM Relationships

3.3.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. Figure 3-5 shows proper termination of the Func Out connector with standard 50Ω output impedance. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch. Termination of the ECL output connector must be 50 ohms into a −2 volts.

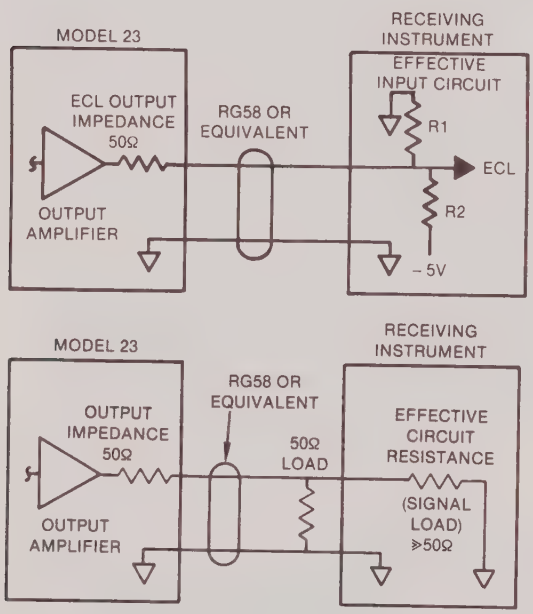


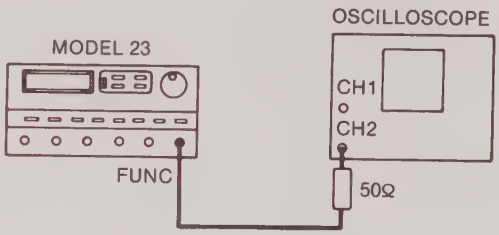
Figure 3-5. Signal Termination

The impedances of the generator input and output connectors are:

Connectors	Impedance
Func Out	50, 75, or 600Ω (Internal jumper selectable or purchased option)
ECL Out	50Ω
TTL Out	50Ω
AM In (600Ω)	600Ω
Trig In (TTL)	One TTL Load
VCG In (10KΩ)	10kΩ

3.3.2 Continuous Operation

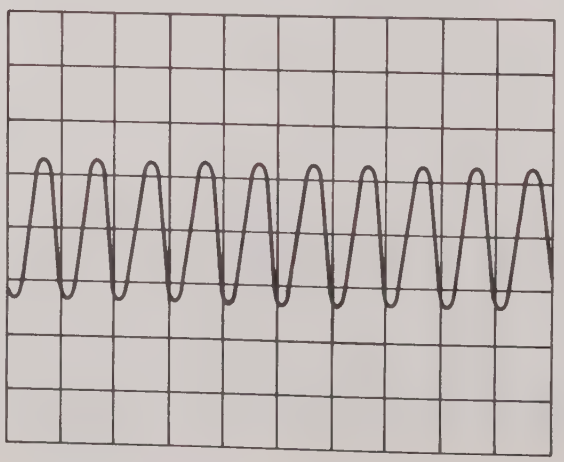
The Model 23 generator will supply a continuous waveform at a fixed frequency as set by the operator, remotely programmed, or by the VCG input connector. This waveform can be sine, triangle, or square wave (up/down ramps also available below 1 kHz). A dc offset is also available for use with these waveforms. To demonstrate continuous operation, connect the Model 23 as shown.



Set the Model 23 controls and the oscilloscope controls as follows:

Model 23	Oscilloscope
Power: On	Vert Input: 2 V/DIV
Reset: Press once	Vert Coupling: DC
	Horiz Sweep: .1 ms/DIV.
	Trig Mode: AUTO
	Trig Coupling: AC
	Trig Source: NORM

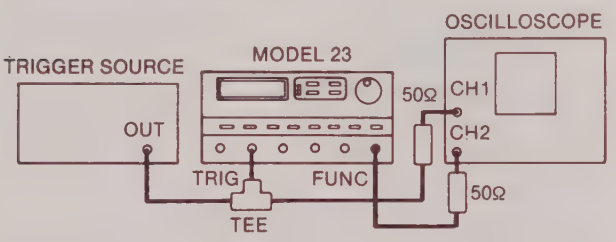
The oscilloscope will display a 10 kHz, 5 Vp-p continuous sine waveform as shown in the following illustration. The frequency can be stepped down (using the left arrow switch) to 10 mHz or up (using the right arrow switch) to 10 MHz. The frequency can be continuously adjusted between 10 mHz and 12 MHz using the Control knob.



3.3.3 Triggered Operation

The Model 23 produces a single complete waveform cycle each time it is triggered. The Model 23 can be triggered by using the Trigger switch on the front panel, by an external trigger signal input at the Trig In (TTL) connector, or by an interface bus command. If a positive trigger slope is selected, the generator is triggered when the switch is pressed. If a negative slope is selected, the generator is triggered when the switch is released. All waveforms may have a dc offset as in continuous mode

To demonstrate external trigger operation, connect the instruments as follows.

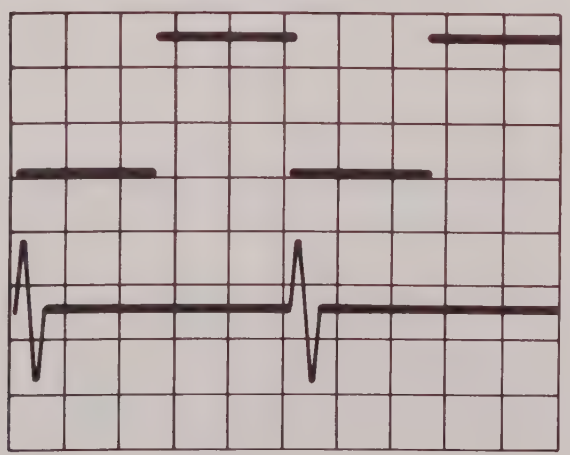


Set the Model 23 controls and the test equipment controls as follows:

Model 23	**Oscilloscope**
Power: On	Vert Input CH1: 1 V/DIV
Reset: Press once	Vert Input CH2: 2 V/DIV
Mode: TRIG	Vert Coupling: DC
Trig Slope: NEG	Horiz Sweep: .2 ms/DIV
	Trig Mode: AUTO
	Trig Coupling: AC
	Trig Source: CH1

Trigger Source
Frequency: 1 kHz
Waveform: Square
Amplitude: 0 to +2.5V (TTL Levels)

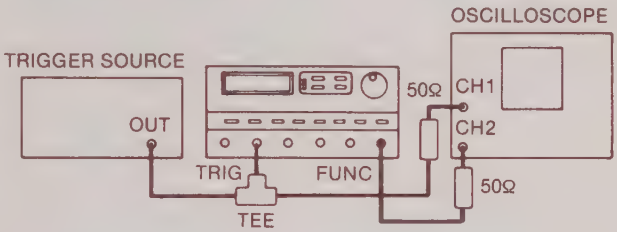
The oscilloscope will display a single cycle of a 10 kHz, 5 Vp-p sine wave each time the trigger waveform goes negative as shown.



3.3.4 Gated Operation

A gated generator produces a continuous output waveform for the duration of the gate trigger signal. The Model 23 can be gated by manual control using the front panel Trigger switch or by means of an external gate trigger at the Trig In (TTL) connector.

To demonstrate external gated operation, connect the instruments as shown.

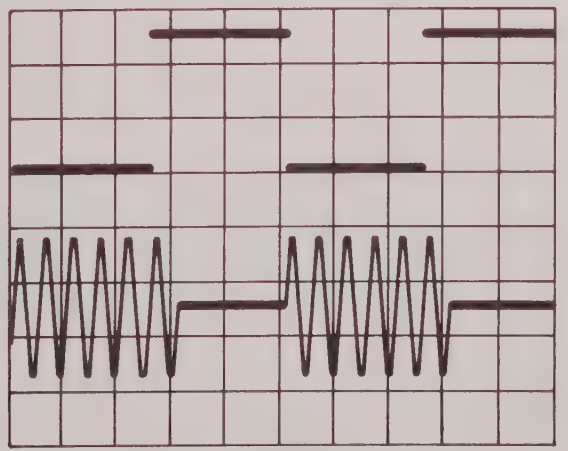


Set the Model 23 controls and the test equipment controls as follows:

Model 23	**Oscilloscope**
Power: On	Vert Input CH1: 1 V/DIV
Reset: Press once	Vert Input CH2: 2 V/DIV
Mode: GATED	Vert Coupling: DC
Trig Slope: NEG	Horiz Sweep: .2 ms/DIV
	Trig Mode: AUTO
	Trig Coupling: AC
	Trig Source: CH1

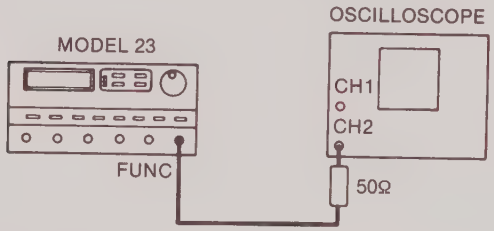
Trigger Source
Frequency: 1 kHz
Waveform: Square
Amplitude: 0 to +2.5V (TTL Levels)

The oscilloscope will display approximately six complete cycles of a 10 kHz, 5 Vp-p sine wave each time the gate trigger waveform goes negative as shown.



3.3.5 Synthesized Operation

The Model 23 synthesized mode provides the same waveforms and frequency ranges as does the continuous mode. *In the synthesized mode the frequency resolution is increased to 4 digits and the accuracy is increased to 0.005% (50 ppm).* The synthesized mode will supply a continuous waveform at a fixed frequency as set by the operator, or programmed by the GPIB. This waveform can be sine, triangle, or square wave (up/down ramps also available below 1 kHz). A dc offset is also available for use with these waveforms. To demonstrate synthesized operation, connect the Model 23 with the indicated test instruments as shown.



Set the Model 23 controls and the test oscilloscope controls as follows:

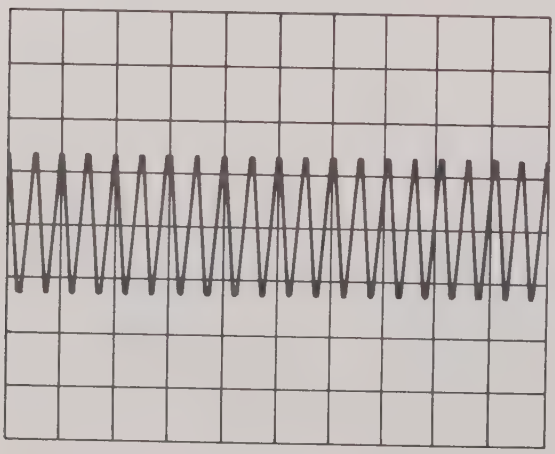
Model 23

Power: On
Reset: Press once
Mode: SYNTH

Oscilloscope

Vert Input: 2 V/DIV
Vert Coupling: DC
Horiz Sweep: .2 ms/DIV.
Trig Mode: AUTO
Trig Coupling: AC
Trig Source: NORM

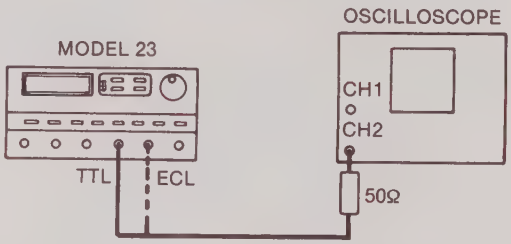
The oscilloscope will display a 10 kHz, 5 Vpp continuous sine waveform as shown in the following illustration. The frequency can be stepped down (using the left arrow switch) to 10 mHz or up (using the right arrow switch) to 10 MHz. The frequency can be continuously adjusted between 10 mHz and 12 MHz using the Control knob.



3.3.6 Clock Mode Operation

In clock mode the function out signal is absent, but the two system square outputs are present as before but in an extended frequency range. The TTL Out connector (TTL level square wave) and the ECL Out connector (ECL level square wave) are both available in this mode over a *range of 10 mHz to 32 MHz.*

To demonstrate the clock mode of operation, connect the Model 23 and the oscilloscope as shown.



Set the Model 23 controls and the oscilloscope controls as follows:

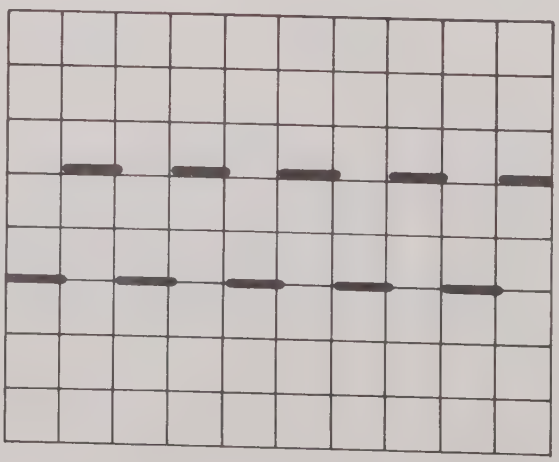
Model 23

Power: On
Reset: Press once
Mode: CLOCK

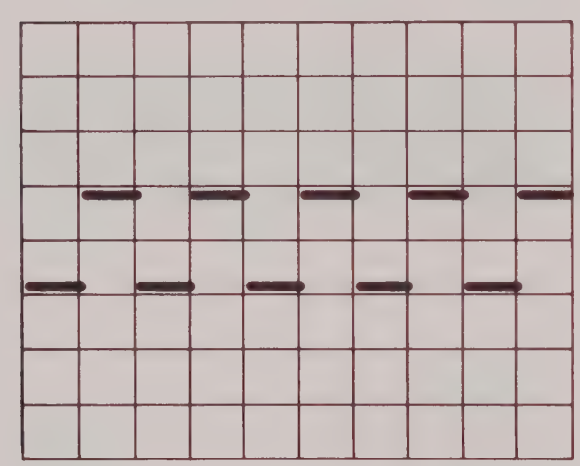
Oscilloscope

Vert Input: 1 V/DIV
Vert Coupling: DC
Horiz Sweep: 50 μs/DIV.
Trig Mode: AUTO
Trig Coupling: AC
Trig Source: NORM

The oscilloscope will display a TTL output square wave (10 kHz at approximately 2 Vp-p) as shown below. The output frequency can be varied in steps (using the left or right arrow switches) or continuously (using the Control knob).



Remove the coaxial cable from the Model 23 TTL Out connector and reconnect to the ECL Out connector. Set the oscilloscope vertical input to 0.1 V/DIV. Readjust the vertical centering if necessary. The oscilloscope will display an ECL output square wave (10 kHz at approximately 0.2 Vp-p) as shown in the following illustration. The ECL Out square wave will not be at ECL levels during this demonstration unless the output is fed into a −2 volt load as in ECL circuits. The waveform shape is representative of the normal ECL loaded output. The output frequency can be varied in steps (using the left or right arrow switches) or continuously (using the Control knob).



3.3.7 Voltage Controlled Generator (VCG) Operation

VCG is an external electronic means of controlling the frequency of the generator. Applying dc voltage levels of up to 0 to + 10V (+ 12V on the top range) or ac signals of up to 10 Vp-p (12 Vp-p on the top range) at the VCG In BNC allows the generator to be swept (up or down in frequency) or frequency modulated.

NOTE

Excessive VCG input voltage may cause nonlinear operation when the generator attempts to exceed the range limits.

3.3.7.1 'Zero' Frequency

In continuous, triggered or gated modes and with frequency selected, the zero switch will set the frequency to the bottom of the current range for 1000:1 VCG change (1200:1 on top range only). The ranges are as follows:

Specified Range* (Programmable Portion)	Lowest Obtainable VCG or "Zero" Frequency
12.00 MHz to 1.00 MHz	10 kHz
999 kHz to 100 kHz	1 kHz
99.9 kHz to 10.0 kHz	100 Hz
9.99 kHz to 1.00 kHz	10 Hz
999 Hz to 100 Hz	1 Hz
99.9 Hz to 10.0 Hz	100 mHz
9.99 Hz to 1.00 Hz	10 mHz
999 mHz to 100 mHz	1 mHz

*See range limitations of each waveform given in section 1.

Frequency Zero is selected by pressing the Freq/Per and Zero keys. The generator frequency sets the 'Zero' frequency which is shown on the top line of the front panel display. The second line shows the frequency change per applied volt at the VCG In connector. For example, if the generator frequency is 5.00 kHz, the specified range is 9.99 kHz to 1 kHz (row 4 in the chart), the 'Zero' frequency is 10 Hz and frequency will vary at a rate of 1 kHz per volt at the VCG In connector. Once in the 'Zero' frequency mode, the generator frequency range, and rate of change can still be modified by pressing one of the front panel arrows or turning the knob.

NOTE

Because range changing is automatic when using the arrows or knob, you may inadvertently change the range in which you wish to VCG.

3.3.7.2 VCG Nomograph

The VCG nomograph in figure 3-6 gives an example of how the input voltage affects the output frequency/range. Applying dc (or dc and ac) at the VCG in connector can produce a 1:1000 sweep in any of the frequency ranges (1:1200 on the top range) according to the following formula:

$$\text{Freq Out} = \text{Freq}_{(\text{programmed})} + \text{Freq}_{(\text{range})} \times {}^{\text{VCG in (V)}}/_{10\text{V}}$$

The V_{FREQ} is always positive (≥ 10 mV), must be less than 12 volts and is the sum of the following formula:

$$\text{Sum} = \text{Freq}_{(\text{programmed})}/\text{Freq}_{(\text{range})} \times 10\text{V} + \text{VCG In}$$

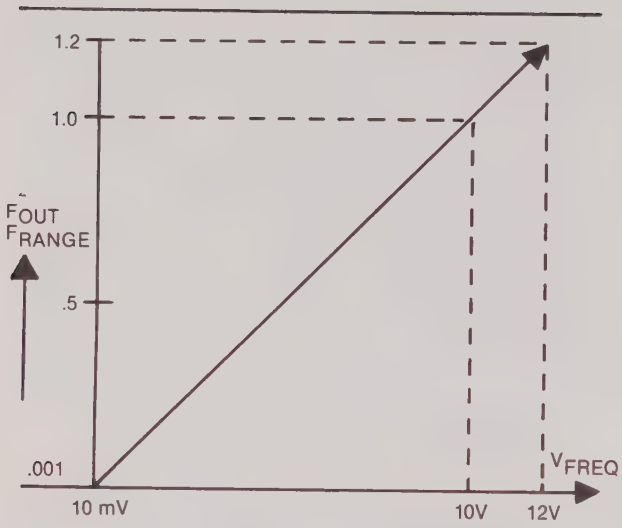
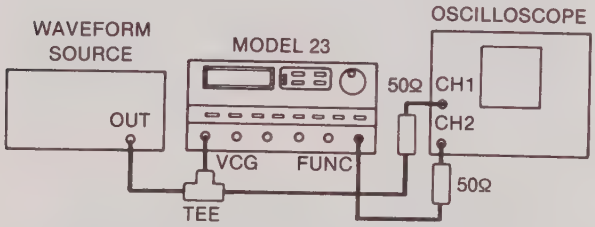


Figure 3-6. VCG Input/Output Relationships

3.3.7.3 Sweep

To demonstrate sweep VCG operation, connect the instruments as shown.



Set the Model 23 and test instrument controls as follows:

NOTE

Because 1000:1 sweep is not being demonstrated, the 'zero' frequency setting is not used.

Model 23

Power: On
Reset: Press once
Frequency: 1.0 kHz

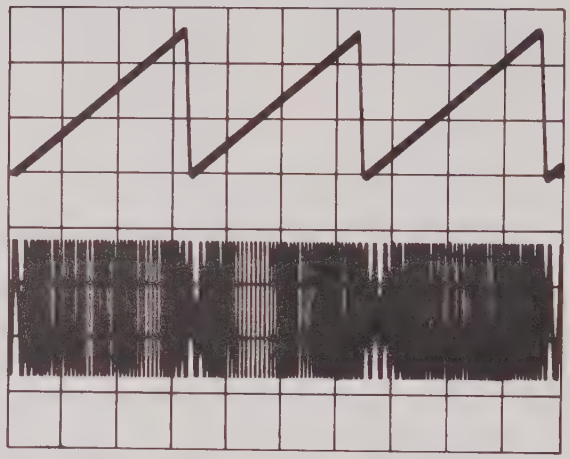
Oscilloscope

Vert Input CH1: 2 V/DIV
Vert Input CH2: 2 V/DIV
Vert Coupling: DC
Horiz Sweep: .5 ms/DIV
Trig Mode: AUTO
Trig Coupling: AC
Trig Source: CH1

Waveform Source

Waveform: Positive Ramp
Amplitude: 0 to +5Vdc
Frequency: 400 Hz

Adjust the waveform source frequency control as necessary to stabilize the Model 23 waveform. Note that in the following illustration the frequency of the Model 23 waveform increases from left to right. The zero amplitude of the ramp signal is the minimum frequency of the Model 23 and that the maximum amplitude of the ramp signal is the maximum frequency of the Model 23.



3.3.7.4 FM

To demonstrate frequency modulation VCG operation, set the Model 23 and test instrument controls as follows:

Model 23

Power: On
Reset: Press once
Frequency: 1.0 kHz

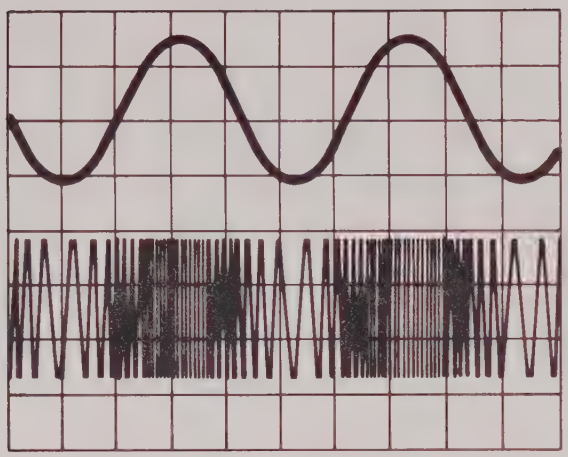
Oscilloscope

Vert Input CH1: 2 V/DIV
Vert Input CH2: 2 V/DIV
Vert Coupling: DC
Horiz Sweep: .5 ms/DIV
Trig Mode: AUTO
Trig Coupling: AC
Trig Source: CH1

Waveform Source

Waveform: Sine Wave
Amplitude: 10 Vp-p (centered at +5 Vdc)
Frequency: 625 Hz

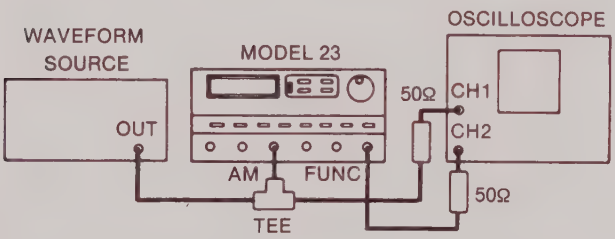
Adjust the waveform source frequency control as necessary to stabilize the Model 23 waveform. Note that in the following illustration the frequency of the Model 23 waveform increases when the sine wave is positive-going and decreases when the sine wave is negative-going. If the Model 23 frequency is set toward the middle of any frequency range, a symmetrical increase above and decrease below the center (display) frequency can be obtained.



3.3.8 AM/SCM Operation

The Model 23 can provide both conventional Amplitude Modulation (AM) and Suppressed Carrier Modulation (SCM) via the AM In (600Ω) connector. An input of 10 Vp-p will provide 100% modulation onto a 5 Vp-p carrier signal. Pressing the Zero switch while in the amplitude display mode will cause the carrier dc amplitude to be zero volts and provide SCM operation via the same AM In (600Ω) connector. The carrier null can be improved by changing the SCM NULL value shown on the Model 23 display. The Control knob will change the value from 0 to a maximum of ±500.

To demonstrate AM operation, connect the instruments as shown.



Model 23

Power: On
Reset: Press once

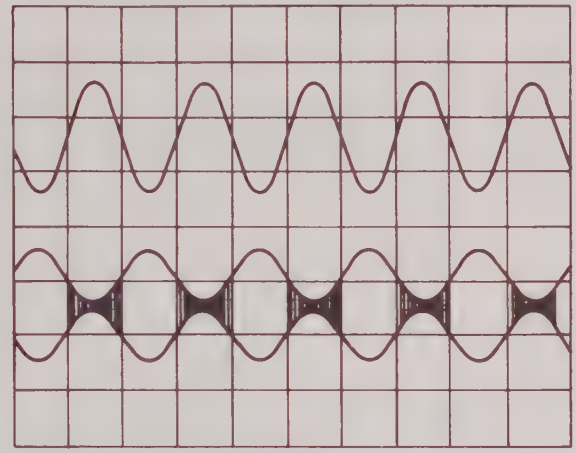
Oscilloscope

Vert Input CH1: 5 V/DIV
Vert Input CH2: 5 V/DIV
Horiz Sweep: .5 μs/DIV
Trig Mode: AUTO
Trig Coupling: AC
Trig Source: CH1

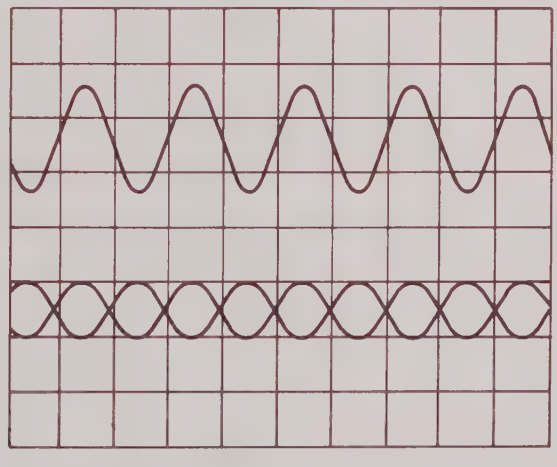
Waveform Source

Frequency: 1 kHz
Waveform: Sine
Amplitude: 10 Vp-p
Frequency: 100 KHz

The oscilloscope will display a 100 kHz continuous waveform carrier 100% modulated at 1 kHz as showm below. Increasing the amplitude of the waveform source will cause overmodulation, while decreasing the amplitude will cause undermodulation.



To demonstrate suppressed carrier modulation, press the Amplitude switch followed by the Zero switch. The oscilloscope will display a suppressed carrier modulation pattern as shown in the following illustration. Adjusting the Control knob will maximize the carrier null.



3.4 THE GENERAL PURPOSE INTERFACE BUS (GPIB)

Paragraphs 3.4 through 3.5 provide background information on the General Purpose Interface Bus (GPIB). For specific Model 23 programming information, refer to paragraph 3.6 through 3.8.2.

The GPIB interface is an implementation of IEEE specification 488-1978. It supports the following interface functions which are described in detail in the

specification. Relevant aspects of these functions are discussed in following paragraphs.

SH1	Complete source handshake.
AH1	Complete acceptor handshake.
T6	Basic talker.
TE0	No extended talker.
L4	Basic listener.
SR1	Complete service request (software select).
RL1	Remote/local and local lockout.
PP0	No parallel poll capability.
DC1	Complete device clear/selective device clear.
DT1	Complete device trigger capability.
E1	Tri-state drivers.

Instruments on the bus may have "talk" and "listen" capabilities. The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

The GPIB consists of 16 negative true signal lines as shown in figure 3-7. hese 16 lines include 8 bidirectional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull up and active pull down. Thus, any device may "assert" a line by pulling it down to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

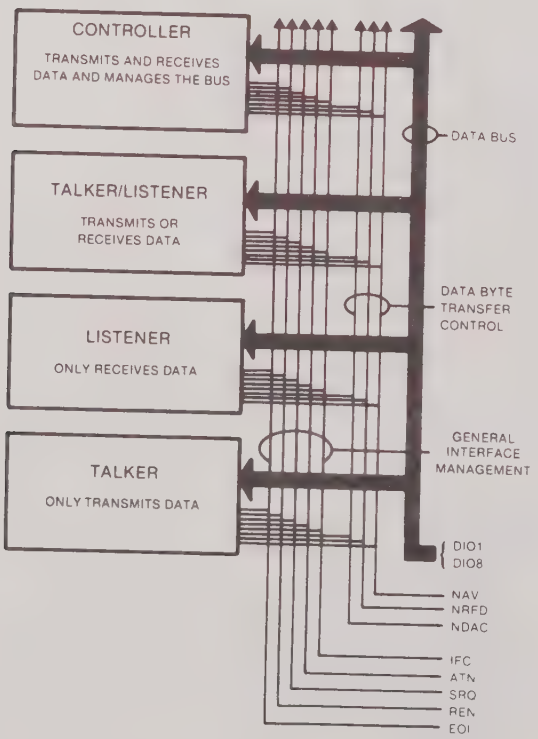


Figure 3-7. GPIB Structure

As shown in figure 3-7, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. More than one controller may be connected to the bus, but only one controller may be hard wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

3.4.1 Bus Line Definitions

The 16 negative-true GPIB signal lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

The functions of the GPIB signal lines are:

DIO1-DIO8 — These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN — The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller originated messages.

REN — The Remote Enable line controls whether devices on the GPIB are in local or remote modes. In the local mode, devices respond to front panel commands. In remote mode, the situation is reversed; GPIB originated commands are obeyed, while front panel commands are ignored. The Model 23 enters the remote state when it receives its listen address and REN is enabled.

The Model 23 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LOCAL front panel soft key is pressed.

DAV, NRFD, NDAC — These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information.

EOI — When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the Model 23 receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When the Model 23 transmits the last byte of a message (which is always a terminator character) it also sets EOI true.

SRQ — The Service Request line is used by the Model 23 and other devices on the bus to signal the controller that they request attention. Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.

IFC — The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.4.2 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as described in the next paragraph.

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.4.3 Commands

Commands are sent over lines DIO1-DIO8 with ATN true. They are divided into five classes:

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands
   - DCL Device Clear
   - SPE Serial Poll Enable
   - SPD Serial Poll Disable
   - LLO Local Lockout
5. Addressed Commands
   - GTL Go To Local
   - SDC Selective Device Clear
   - GET Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A.

3.4.3.1 Listen Address

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes SP through ►). Unlisten (address "32", hexadecimal "3F", ASCII "?") is used to command all devices to not read data bytes. The Wavetek Model 23 listen address is selected by internal switches (figure 2-7) or by front panel keyboard. To temporarily change the GPIB address, press the front panel status key until GPIB ADRS appears in the display. Then turn the knob until the current address is displayed. At power on, the address always matches the internal switches.

3.4.3.2 Talk Address

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 40 through 5E, ASCII codes @ through ↑). A 32nd address, called untalk (hexadecimal 5F, ASCII "_") is used to command all devices to cease talking. The lower 5 bits of the Model 23 talk address are selected by the same switches used to select the listen address. Thus, if the Model 23 listen address is hexadecimal 21 (ASCII "!"), the talk address is hexadecimal 41 (ASCII "A").

3.4.3.3 Secondary Address

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the Model 23.

3.4.3.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Model 23 are:

1. Device Clear (DCL) — Resets the Model 23 to the default settings. DCL affects all devices on the bus.
2. Serial Poll Enable (SPE) — Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to all zeros, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the Model 23 talk message number 1. When this message is read, the status byte is reset and the SRQ released as for the serial poll.
3. Serial Poll Disable (SPD) — Discontinues serial poll. Returns instrument to normal talk modes.
4. Local Lockout (LLO) — Causes the Model 23 to enter a state where the front panel LOCAL soft key is inoperative. In this state the instrument will only accept parameter changes through the GPIB. To enable parameter changes, the GPIB controller can send the GTL (Go To Local) command.

3.4.3.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the Model 23 are:

1. Go To Local (GTL) — Commands the Model 23 to go to the local mode.
2. Selective Device Clear (SDC) — Resets the Model 23 to its default conditions. SDC affects only the selected unit.
3. Group Execute Trigger (GET) — Upon receipt of the GET, the programmed settings are error checked. If no error is detected, the control information is transferred to the waveform generator circuit, followed by a trigger pulse from the microprocessor.

3.5 DATA TRANSFER

The Model 23 is programmed by first sending the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 124 characters are received or there is a pause during the transfer of data. At the time, the entire string of received characters is scanned by the microprocessor, which carries out the scan and accepts the next 124 character string. Whenever the microprocessor is finished scanning a string, the display will show the last parameter of the string and the current status of the GPIB interface. If the EOI line is asserted while sending a character to the Model 23, the currently programmed terminator character will be put into the input string following the character with the EOI.

In addition to accepting programming characters, the Model 23 will transmit status information over the bus.

3.6 MODEL 23 GPIB PROGRAMMING

This section describes the remote operation of the Model 23. For instrument description and local operation, refer to paragraphs 3.1 through 3.3.8. For general GPIB programming information, refer to paragraph 3.4 through 3.5

Paragraphs 3.6.1 through 3.6.6 provide background information and should be read before attempting to program the Model 23. Table 3-2 is a programming reference guide giving detailed descriptions of each programming character and information for writing actual statements to the Model 23.

3.6.1 General Programming Information

When the instrument is in remote, the GPIB interface input has priority over any front panel control, and the knob is completely ignored. Therefore, if the GPIB interface is continuously supplied with data, the keyboard will appear to be inoperative to the user.

Line 1 of the LCD display always shows the state of the GPIB interface after scanning the last string (see paragraph 3.5). In the upper right corner, several characters may appear:

R = Remote
L = Addressed to listen
T = Addressed to talk
Q = Request of service because of selected SRQ mode

Line 2 is the parameter and special message readout. An asterisk to the left of the parameter indicates that an execute has not been sent.

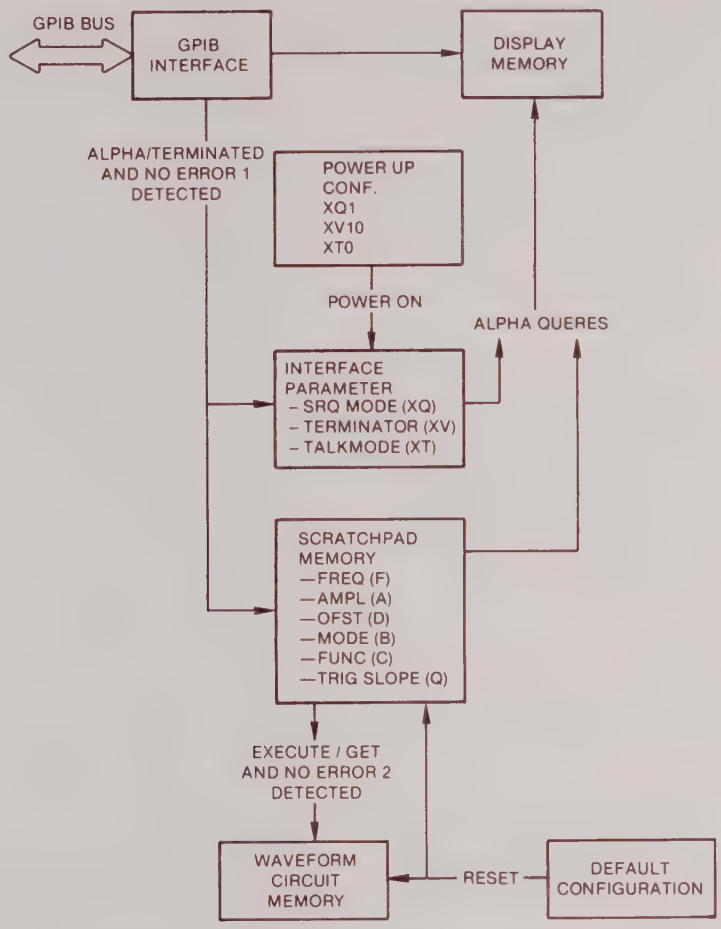


Figure 3-8. GPIB Memory Structure and Data Flow

The front panel display is externally programmed by sending any ASCII character between single quotes ('test string) or double quotes ("test string").

3.6.2 Basic Command Structure

The Model 23 is programmed by sending ASCII coded characters to the instrument (see table 3-2 and Appendix A). Figure 3-8 gives an overview of the internal memory structure and data flow.

3.6.3 Characters

There are 5 types of characters that can be sent over the GPIB bus. These are:

Alphabetic characters. A through Z (except E). These select action or parameter commands. Both upper and lower case characters are accepted.

Numeric characters (Suffix). These are 0 through 9, E (exponent), – (negative) and the decimal point. They control the selected parameter.

Special characters. The instrument will order any set of characters within single or double quotes, such as 'string' or "string" to the display.

Nonprogramming characters. These are characters not in one of the previous described classes. They have no effect on programming and may be interspersed freely after any programming character other than X.

Terminator. Designates the end of a character string. Initially, this is line feed (LF).

3.6.4 Action and Parameter Commands

The alphabetic characters are used to select either actions or parameters. Four characters select action commands. These cause an immediate action when sent

and do not require entry of a numeric suffix. The remaining alphabetic characters are parameter commands and require one or two letters plus a numeric suffix to control some aspect of the instruments operation.

3.6.5 Action Commands

Action commands which cause an immediate action when sent and do not require entry of a numeric suffix are:

"J" (Manual trigger asserted)
"H" (Manual trigger unasserted)
"I" (Execute)
"Z" (Reset)

To program an action, simply send the proper alphabetic character to the GPIB interface. For example, to reset the Model 23, simply send the letter "Z". The action will then take place, but only if the instrument is in the enable state when the character is read by the microprocessor. See paragraph 3.4.1 REN (Remote Enable) for further information.

3.6.6 Programming Parameters

Parameter commands require one or two letters plus a numeric suffix to control some aspect of the instruments operation.

There are only two exponent digits allowed. Only one decimal point and one E (exponent) are allowed per number, all others are ignored. Any number of non-programming characters may be interspersed with the numeric suffix as they have no effect.

To examine the current value of a parameter, simply program the proper alphabetic character (F = frequency etc.). If the parameter is legal, the current value will be displayed on the instrument front panel along with an asterisk (*) until the parameter is executed.

To change a parameter value, first program the alphabetic character which selects the desired parameter. Next, program the new value using numeric characters (0 through 9, E, −, .). Data entry can be fixed point, floating point, exponential notation or scientific notation. Any sequence of characters which gives the new value is acceptable. For example, all of the following sequences cause frequency 100 Hz to be programmed.

Programming String for Frequency 100 Hz	Remarks
F 100	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E-2-	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the number input format is so general, the instrument must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic character, a special character, or a terminator character. When this is done, the new value is rounded off (see table 3-1) and tested to see if it is a legal value for the setting being changed. If it is legal, the new value will then be entered into the instruments scratchpad memory.

If an execute (I) has not been sent and the new value is different from the parameter in the scratchpad memory, an asterisk (*) is shown on the display (see paragraph 3.6.1). After an I (execute) or a GET command is sent, all the parameters in the scratchpad are checked for interparameter conflicts and if no error occurs the scratchpad contents are transferred to the waveform memory (see table 3-1). An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.

It is also possible to send multiple commands in the same string. For example, to change frequency, amplitude and offset simultaneously, send the parameter string: "F1E4A2D1I". In this example, the new frequency is 10 kHz, amplitude is 2 Vp-p and offset is 1V. Because an execute was sent at the end of this string, the parameter changes are executed immediately.

3.6.7 Programming Reference Guide

Table 3-2 can be used as a programming reference guide when writing actual statements to the Model 23. It describes each programming character and which numeric characters are to be used to program parameter values. Before attempting to use this guide, read paragraphs 3.6.1 through 3.6.6.

When programming the Model 23, keep in mind that at initial power up, the following remote settings have been defaulted.

Function	ASCII Character	Default Setting
GPIB ADRS	—	Bit Switch
SRQ Mode	XQ	1
Talk Mode	XT	0
Terminator Select	XV	10

Table 3-1. Parameter Round Offs

	Round Off Values (Scratchpad Input)		Execute Round Off Values (Scratchpad to Waveform Memory)		
Parameter	**Range***	**Round Off**	**Mode**	**Range**	**Round Off**
Frequency	0.01 Hz to <10 MHz	4 Digits	Synth	0.01 Hz to 12 MHz	No Round Off
	10 MHz to <16 MHz	5 Digits	Clock	0.01 Hz to 32 MHz	No Round Off
	16 MHz to 32 MHz	5 Digits (Up to Next Even LSD)	All Others	0.01 Hz to <10 MHz	3 Digits
				10 MHz to 12 MHz	4 Digits
Amplitude**	10 mVp-p to <10 Vp-p	3 Digits or Nearest 0.1 mVp-p			
	10 Vp-p to 10.2 Vp-p	4 Digits or Nearest 10 mVp-p			
Offset**	−5.1V to +5.1V	3 Digits or Nearest 0.1 mV			
Ampl Vp-p + 2 (Absolute Offset)				10 mVp-p to <0.1 Vp-p	3 Digits or Nearest 0.1 mVp-p
				0.1 Vp-p to <1 Vp-p	3 Digits or Nearest 1 mVp-p
				1 Vp-p to 10.4 Vp-p	Nearest 10 mVp-p
Remaining Parameters		To Closest Integer			None

*Values not shown are invalid.
**Terminated into 50Ω.

Table 3-2. Programming Reference Guide

Function	ASCII Character(s)	Description
Amplitude	A	An A followed by a number value programs the peak to peak amplitude into the correct impedance at the Func Out connector. Valid amplitude values are 10E-2 to 10.2. For rounding off, refer to table 3-1.
Amplitude Zero (SCM)	A0	Zeros or nulls both the output amplitude and offset. Also allows for suppressed carrier modulation. Any future offset programming while in SCM is ignored.
Execute	I	An action command that causes all parameters in the scratchpad to be checked for interparameter conflicts. If no error is found, the rounded scratchpad contents are transferred to the waveform memory. An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.
Exponent	E	Designates the numerals immediately preceding "E" to be raised by the *10 power of the following numeral and ± entries. For example, F3E-1 = Frequency 3* 10^{-1} = Frequency 0.3 Hz.
Frequency	F	An F followed by a number value programs the generator frequency in hertz. For rounding off, refer to table 3-1. An "E" designates exponent. Valid frequency values are: Clock Mode 10E-2 to 32E6 Cont/Trig/Gate/Synth Mode 10E-2 ... 12E6 Trig Hav/Gate Hav Mode 10E-2 to 999 Sine/Square/Triangle Func 10E-2 to 12E6 Ramp Up/Ramp Dn Func 10E-2 to 999(.9)
Frequency Zero (FM)	F0	Sets the output frequency to the lower end of the selected frequency range (see paragraph 3.3.7.1). This range is determined by programming a frequency within the limits of that range before programming F0.
Function	C	The character C followed by a single digit code between 0 and 5 selects function at the Func Out connector. FUNCTION CODE Sine wave C0 Square wave C1 Triangle wave C2 Ramp Up C3 Ramp Dn C4 DC C5

Table 3-2. Programming Reference Guide (Continued)

Function	ASCII Character(s)	Description
Mode	B	The character 'B' followed by a single digit code between 0 and 4 selects the operating mode of the instrument..
		MODE — **CODE** Continuous — B0 Triggered — B1 Gated — B2 Triggered Haver (F<1E3 not valid for Ramp Up or Ramp Dn) — B3 Gated Haver (F<1E3 not valid for Ramp Up or Ramp Dn) — B4 Clock (10 mHz to 32 MHz only valid for sync out signals) — B5 Synthesized (same as continuous but with increased frequency accuracy — B6
Number Character	0-9, ±, .	The numeric characters (0 through 9, E, −) are used to program new parameter values. Data entry is free format, i.e., fixed point, floating point and exponential notation, or scientific notation. Fixed Point: Decimal remains at far right. Floating Point: You program the decimal point. It floats to the left in its designated position as you enter more numerals. Exponential Notation: A value, then E followed by the exponent of a times ten multiplier. When the value (mantissa) is limited to one digit, exponential notation is called scientific notation.
Offset	D	The Character D followed by a number value programs the offset voltage into the correct impedance at the Func Out connector. Valid offset values are −5.1 to +5.1. For rounding off, refer to table 3-1.
Reset	Z	An action command that sets the waveform and scratchpad memories to the defined default values. Refer to paragraph 3.2 number 21 for the initial values.
Trigger		In remote operation, triggered and gated modes of the generator are initiated by an external signal at the Trig In connecter, or the J and H commands via the GPIB.
Man. Trig. Pressed	J	See following Triggering/Gating Chart.
Man. Trig. Released	H	See following Triggering/Gating Chart.

Table 3-2. Programming Reference Guide (Continued)

<table>
<tr><th>Function</th><th>ASCII Character(s)</th><th>Description</th></tr>
<tr><td>Trigger Slope</td><td>Q</td><td>The character 'Q' selects generator triggering or gating on the rising or falling edge of the Trig In (TTL) signal or GPIB 'J' (positive slope) or 'H' (negative slope) command. See TRIGGERING/GATING CHART below.

TRIGGERING/GATING CHART
<table><tr><th></th><th>Positive Slope (Rising Edge) Q0</th><th>Negative Slope (Falling Edge) Q1</th></tr><tr><td>J</td><td>Trig: Single Cycle
Gate: Freeruns</td><td>Trig: Reset
Gate: Off</td></tr><tr><td>H</td><td>Trig: Reset
Gate: Off</td><td>Trig: Single Cycle
Gate: Freeruns</td></tr></table></td></tr>
<tr><td>SRQ Mode</td><td>XQ</td><td>XQ followed by a value ("0" to "255") selects the conditions under which the Model 23 asserts the SRQ line on the GPIB bus and sets the rsv bit in the serial poll response byte. The equivalent binary value is a "mask" for the serial poll response byte. All undefined bits will have no effect if selected.

<table><tr><th>BIT VALUE</th><th>DESCRIPTION</th></tr><tr><td>0000 1000</td><td>Battery backup level low</td></tr><tr><td>0000 0001</td><td>Class 1 or 2 program error</td></tr><tr><td>0000 0010</td><td>Execute Completed</td></tr></table>
Serial Poll Response Bit
<table><tr><th>128</th><th>64</th><th>32</th><th>16</th><th>8</th><th>4</th><th>2</th><th>1</th></tr><tr><td>Undef'd</td><td>rsv</td><td>Undef'd</td><td>Undef'd</td><td>Batt Low</td><td>Undef'd</td><td>Exec Compt'd</td><td>Program Error</td></tr></table>
Each bit value represents a condition that, if selected by the SRQ mode, will represent the GPIB's SRQ line and the SERIAL POLL byte's rsv bit. Each bit may be selected individually or in various combinations.

Examples:

XQ1 asserts the SRQ line and rsv bit when there is a program error such as "offset" beyond the Model 23 limits.

XQ9 initiates a service request if either a program error has occurred or the battery voltage is detected low after receiving a reset command (Z) or device clear command.</td></tr>
<tr><td>Talk Mode</td><td>XT</td><td>To read a message from the Model 23, send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Mode (XT) setting. The last character of the Model 23's message will be the currently programmed terminator character with the EOI line asserted.

XT followed by a code (0 through 5) selects the kind of message the 23 will send when it is addressed as a talker on the GPIB.</td></tr>
</table>

Table 3-2. Programming Reference Guide (Continued)

Function	ASCII Character(s)	Description
		Code Message XT0 Programming error list. A typical error string is E 1F 2AD. Some error string characteristics are: A. All error strings begin with E B. Most recent error is at the end of the string C. Errors are separated by space D. Class 1 error: A 1 followed by the programming character that caused the error (example 1F) E. Class 2 errors: A 2 followed by the two conflicting parameters F. Error strings can be up to 80 characters in length H. After transfer, the instrument clears the error string. XT1 Poll Byte response: The byte (see paragraph 3.4.3.4) that is sent if a serial poll was performed. The controller, by reading this byte, causes the instrument to clear the poll byte and reset the SRQ line if asserted. XT2 The most recently selected parameter and its value. Example: Freq 1.23E3. If no parameter is selected, the instrument returns NO PARAMETER SELECTED. XT3 The entire instrument setup after last execute. Example: F10E3 A5 D0 C0 Q0. XT4 The entire instrument setup when execute is received; same format as XT3. XT5 Instrument identification: Wavetek Model 23 V(X.Y). X.Y identifies the software version number.
Terminator Select	XV	At power on time, the terminator or End of String (EOS) character (see EOI description, paragraph 3.4.1) is the ASCII line feed LF. If the GPIB controller does not look for the end message (EOI line low), and it does not recognize the line feed (LF) as a string terminaor, a new EOS character will be needed. The EOS terminator may be changed to any ASCII character (except NUL) by sending XV followed by the decimal value (argument) corresponding to the new terminator. Example: XV13 changes EOS character to carriage return (CR). XV0 as a special case means that the instrument will accept and send 'C_R or 'L_F' and send 'CR' and 'LF' as a terminator.

3.7 MODEL 23 GPIB CONTROLS

GPIB instrument address, local control and command recall are controlled at the Model 23.

3.7.1 GPIB Address

At power on, the bit switch (figure 2-7) selects the GPIB ADRS (address) value. This value may be changed from the front panel. To do this, first press the status button until GPIB ADRS appears, then rotate the knob until the desired address is displayed. At power off the address returns to the bit switch setting.

3.7.2 GTL (Trigger) Key

If the unit is in remote mode, the Trigger key is actually the GTL (Go To Local) key. Pressing this key brings the Model 23 into local control providing the controller has not locked out the key (see paragraph 3.6.1).

3.7.3 CMD RCL Key (◄►)

For units with any remote option, the ◄ and ► keys are also the CMD RCL (Command Recall) keys. Pressing either one of these keys while in remote displays the last 16 ASCII characters received by the GPIB interface. The previously received characters can be scrolled on the display by spinning the control knob. A pointer on the display indicates the position of the viewing window relative to the last received character. Any nonprintable ASCII character except C_R and L_F are displayed as dots. This feature can be used as a debugging tool for remote instrument programming.

3.8 ERRORS

When an illegal value is programmed or interdependent parameter errors are detected, an error signal is indicated on the GPIB. The service request line is asserted if the service mode (XQ) has been selected (see SRQ description, paragraph 3.4.1). The controller can then serial poll its instruments to locate the source of the service request. It then inquires as to the nature of the request. The method of reporting errors on the GPIB is given in table 3-2 (SRQ Mode).

3.8.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the selected parameter. For example, programming an amplitude of 500 volts will cause a parameter error when the next alpha character is programmed. At this time, the Model 23 disregards the new value and retains the previously programmed value in scratchpad memory.

Example:

After receiving a frequency value, a round off (see table 3-1) is made followed by the limit test 10E-3 to 32E6. Any value outside these boundaries causes a class 1 error.

Table 3-3. Class 1 Error Guidelines

This Parameter	Must (After Rounding) Be Within:
Amplitude	$10*10^{-3}$ and 10.2 (Or "0" for SCM)
Offset	−5.1 and +5.1
Frequency	$10*10^{-3}$ and $32.000*10^{6}$ (Or "0" for FM)
Mode	0 and 6
Function	0 and 5
Trigger Slope	0 and 1
SRQ Mode	0 and 255
Talk Message	0 and 5
Terminator	0 and 127

3.8.2 Class 2 Errors

Class 2 errors are interparameter inconsistencies such as 2*ABS(OFST) + peak to peak amplitude greater than 10.4V. Figure 3-9 shows the possible types of class 2 errors. Tests are made every time an execute (I) or GET is given. If no class 2 error is detected, all scratchpad values are transferred to the waveform memory (see table 3-1).

Note that when an Execute (I) or GET is performed, and the programmed frequency value stil doesn't satisfy the frequency mode/func relation, an error 2 is detected and none of the scratchpad values are executed.

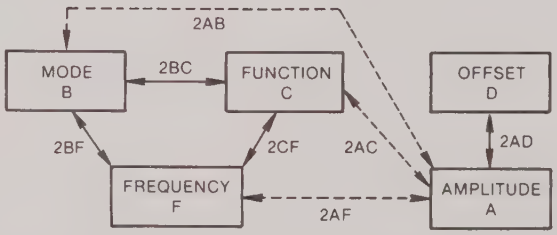


Figure 3-9. Class 2 Errors

2AB A = 0 (SCM) and Mode = Clock

2AC A = 0 (SMC) and Function = DC

2AD Ampl p-p + 2 * ABS (OFST) > 10.4V

2AF A0 and F0 selected (SCM and FM simultaneously)

2BC	Mode	Function
	Trig Hav (B3)	Ramp Up (C3)
	Gate Hav (B4)	Ramp Dn (C4)
	Trig Hav (B3)	Ramp Dn (C4)
	Gate Hav (B4)	Ramp Up (C3)
	Clock (B5)	DC (C5)

2BF	Mode	Frequency
	Cont (B0)	F > 12.00 MHz
	Trig (B1)	F > 12.00 MHz
	Gate (B2)	F > 12.00 MHz
	Trig Hav (B3)	F > 999 Hz
	Gate Hav (B4)	F > 999 Hz
	Synth (B6)	F > 12.00 MHz
	Clock (B5)	F0 (FM)
	Synth (B6)	F0 (FM)

2CF	Function	Frequency
	Sine (C0)	F > 12.00(0) MHz and not Clock Mode
	Square (C1)	F > 12.00(0) MHz and not Clock Mode
	Triangle (C2)	F > 12.00(0) MHz and not Clock Mode
	Ramp Up (C3)	F ⩾ 1 kHz and not Clock Mode
	Ramp Dn (C4)	F ⩾ 1 kHz and not Clock Mode
	DC (C5)	F0 (FM)

3.9 GENERAL RS-232-C INFORMATION

EIA standard RS-232-C specifies the electrical characteristics and pin out of a serial communication standard for connecting "data terminal equipment" (DTE) to "data communication equipment" (DCE). Data terminal equipment is usually devices such as terminals, computers, or printers that are the final destination for data. Data communication equipment, on the other hand, is usually a modem or other device that converts the data to another form and passes it through. Because RS-232-C signal lines defined as inputs on a DCE device are outputs on a DTE device and vise versa, connection to another DCE or of a DTE to another DTE will require a special cable with many of the signals interchanged. These cables are often called "modem eliminators" because they are used to eliminate a pair of modems between two computers. The Model 23 can be configured as either a DCE or DTE device, so in most cases it can be connected with a straight through cable to either a computer or to a modem.

The baud rate is the bit rate during the transmission of a word in bits per second. Different devices use many baud rates but the baud rates of the two devices that are connected must be the same. The Model 23 can be set to 13 different baud rates ranging from 50 to 9,600 as shown in table 2-5.

Data signals over the RS-232-C use a voltage of + 3 to + 25V to represent a zero (also called a space) and a voltage of − 3 to − 25V to represent a one (also called a mark). Handshake and control lines use + 3 to + 25V to indicate a true condition and − 3 to − 25V to indicate a false condition.

When no data is being transmitted, the idle state of the data lines will be the mark state. To transmit a byte, the transmitting device first sends a start bit which is a space for one bit time (1/baud rate) to synchronize the receiver. Next, the data bits are sent LSB first (the Model 23 uses 8 data bits), then at least one bit time of the mark state (stop bits) before initiating the transmission of the next byte. Some devices use an optional parity bit between the data bits and the stop bits. The Model 23 does not support this and it should be suppressed on the connected device (see figure 3-10).

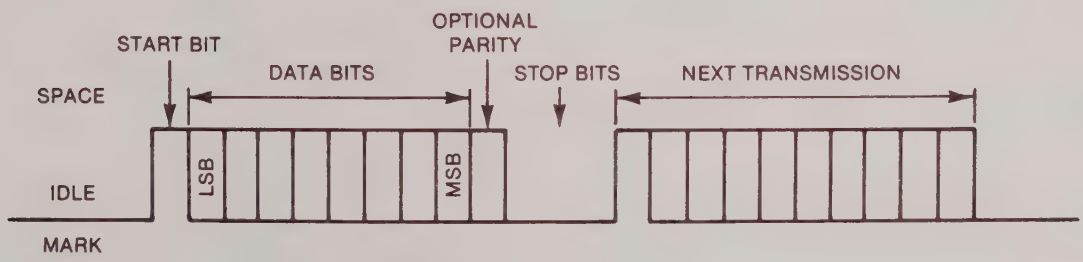


Figure 3-10. Transmission Example

The RS-232-C standard is not very specific about many of the handshaking signals and it is therefore usually necessary to refer to the manuals for both of the devices being connected to determine the exact pin out, signal definition, and signal direction for the devices (see paragraph 2.2.7, 2.2.8, and table 2-4) for the Model 23 pin outs).

Handshaking is used so that each device can tell the other device when it is ready or not ready to receive data. The Model 23 supports two different types of handshaking, **CTS/DTR** (hardware handshaking) and **XON/XOFF** (software handshaking), (see table 3-5). With hardware handshaking, the DCE device pulls the CTS line positive or negative to indicate whether it is ready or not ready respectively and the DTE device pulls the DTR line positive or negative to indicate whether it is ready or not ready respectively. With XON/XOFF handshaking either device sends and XOFF ($13) over the appropriate data line when it is no longer ready to receive data, then sends an XON ($11) when it is again ready.

When the Model 23's DTR (DCE configuration) or CTS (DTE configuration) line is pulled negative, it will send a maximum of one character before it stops transmitting and waits for the handshake line to return positive. When the Model 23 receives an XOFF character it will send a maximum of 3 characters before it stops transmitting and waits to receive an XON character.

When the Model 23's internal buffer fills, it will do one of two things depending on the handshaking mode set from the HAND soft key. If the handshaking mode is CTS/DTR, the Model 23 will set the CTS line negative if it in the DCE configuration or set the DTR line negative if it is in the DTE configuration. When the Model 23 is again ready to receive data it will set the appropriate line back positive. If the handshaking mmde is set to XON/XOFF, the Model 23 will send an XOFF character over the data line. When it is again ready to receive data it will send an XON. After the Model 23 either sets the handshake line negative or sends the XOFF, the connected device must stop sending data within 10 characters or data will be lost.

The SRQ mode (XYn) has no effect over the RS-232-C interface, however the serial poll byte can be read using talk mode (XT1).

When the instrument is in the remote mode (sending the ASCII character '!' causes the instrument to go to remote), the SERIAL interface input has priority over any front panel control, and the Control knob is completely ignored. Therefore, as long as the SERIAL interface is continuously supplied with data, the keyboard will appear to be inoperative to the user.

Line 1 of the LCD always shows the state of the SERIAL interface after scanning the last string. In the upper right corner, a character will appear:

'R' = Remote (if the unit is in remote)

Line 2 is the parameter and special message readout. An asterisk to the left of the parameter indicates that an execute has not been sent.

The front panel display is externally programmed by sending any ASCII character between single or double quotes, such as 'test string' or "test string".

The Model 23 is programmed by sending ASCII coded characters to the instrument (see table 3-6 and Appendix A).

3.9.1 Basic Command Structure

Figure 3-11 gives an overview of the internal memory structure and data flow.

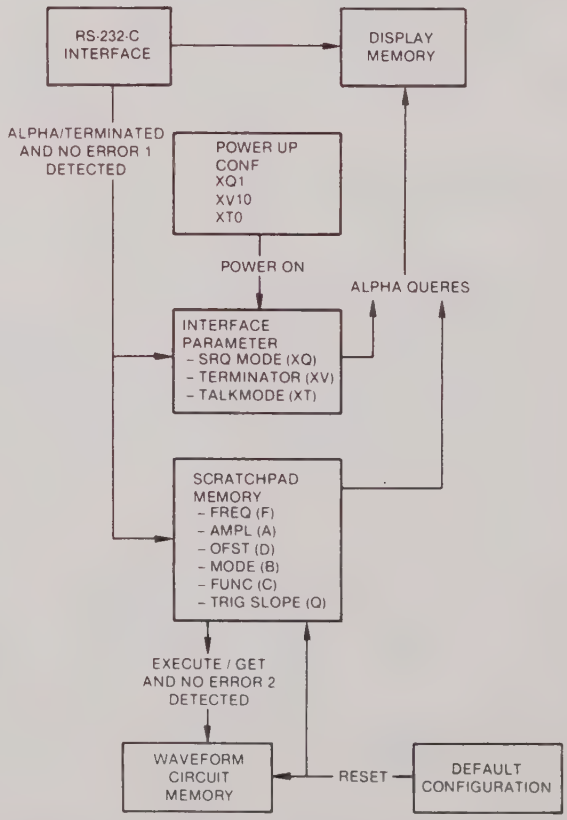


Figure 3-11. RS-232-C Memory Structure and Data Flow

3.9.2 Characters

There are 6 types of characters that can be sent over the SERIAL bus. These are:

Alphabetic characters. 'A' through 'Z' (except 'E'). These select action or parameter commands. Both upper and lower case characters are accepted.

Numeric characters (Suffix). These are '0' through '9', 'E' (exponent), '−' (negative), '+' (positive), and the decimal point. They control the selected parameter.

Special characters. The instrument will display any set of characters within single or double quotes, such as 'string' or "string".

Interface control characters. These are the characters '!', '*', '$', '?', 'DC1' (XON), and 'DC3' (XOFF).

Nonprogramming characters. These are characters not in one of the previous described classes. They have no effect on programming and may be interspersed freely after any programming character other than 'X'.

Terminator. Designates the end of a character string. Initially, the instrument will accept a 'CR' or a 'LF' and send a 'CR + LF' as a terminator.

3.9.3 RS-232-C Terminators

Upon "power-on", the Model 23 accepts either a carriage return (CR) or a line feed (LF) as an end of string (EOS) terminator and sends both a CR and LF as the EOS terminator. If the connected device does not recognize either one, the terminator will need to be changed. The terminator can be changed to any interface control characters or ASCII character other than DC1 (XON) and DC3 (XOFF), or NULL by sending 'XV' followed bny the decimal ASCII code for the character. A terminator code of '0' is a special case and represents the default condition of sending a CR and LF and accepting either CR or LF as previously mentioned.

3.9.4 Action and Parameter Commands

The alphabetic characters are used to select either actions or parameters. Nine characters select action commands. These cause an immediate action when sent and do not require entry of a numeric suffix. The remaining alphabetic characters are parameter commands and require one or two letters plus a numeric suffix to control some aspect of the instruments operation.

3.9.5 Action Commands

Action commands which cause an immediate action when sent and do not require entry of a numeric suffix are:

'J' (Manual trigger pressed)
'H' (Manual trigger released)
'I' (Execute)
'Z' (Reset)

To program an action, simply send the proper alphabetic character to the SERIAL interface. For example, to reset the Model 23, simply send the letter 'Z'. The action will then take place, but only if the instrument is in the remote state when the character is received by the instrument.

3.9.6 Programming Parameters

Parameter commands require one or two letters plus a numeric suffix to control some aspect of the instruments operation

There are only two exponent digits allowed. Only one decimal point and one 'E' (exponent) are allowed per number, all others are ignored. Any number of non-programming characters may be interspersed with the numeric suffix as they have no effect except for the interface control characters.

To examine the current value of a parameter, simply program the proper alphabetic character ('F' = frequency etc.) If the parameter is legal, the current value will be displayed on the instrument front panel along with an asterisk (*) until the parameter is executed.

To change a parameter value, first program the alphabetic character which selects the desired parameter. Next, program the new value using numeric characters ('0' through '9', 'E', '+', '−', and '.'). Data entry can be fixed point, floating point, exponential notation or scientific notation. Any sequence of characters which gives the new value is acceptable. For example, all of the following sequences cause sample frequency 100 Hz to be programmed.

Programming String for Frequency 100Hz	Remarks
F 100	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E-2-	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the number input format is so general, the instrument must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic character, a special character, or a terminator character. When this is done, the new value is rounded off (see table 3-4) and tested to see if it is a legal value for the setting being changed. If it is legal, the new value will then be entered into the instruments scratchpad memory.

Some parameters require that they be followed by an execute (I). If an execute (I) has not been sent and the new value is different from the parameter in the scratchpad memory, an asterisk (*) is shown on the display. After an 'I' (execute) command is sent, all the parameters in the scratchpad are checked for conflicts and if no error occurs the scratchpad contents are transferred to the waveform memory (see table 3-4). An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.

3.9.7 Programming Reference Guide

Table 3-6 can be used as a programming reference guide when writing actual statements to the Model 23. It describes each programming character and which numeric characters are to be used to program parameter values. Before attempting to use this guide, read paragraphs 3.9 through 3.9.6.

Table 3-5 describes the specific interface control commands, while table 3-6 can be used when writing serial statements to the Model 23.

When programming the Model 23, keep in mind that at initial power up, the following functions are at their default settings.

Function	ASCII Character	Default Setting
BAUD RATE	—	Bit Switch
Talk Mode	XT	0
Terminator Select	XV	0

3.10 RS-232-C CONTROLS

The RS-232-C controls listed in paragraphs 3.10.1 thru 3.10.4 are referenced to figure 3-12, RS-232-C Controls and Switches.

3.10.1 Baud Rate Switch (1)

Changing the position of each individual switch section (and therefore the overall combination) in the Baud Rate switch produces a different Baud Rate for the serial port. The Baud Rate set by this switch is the unit default value. See table 2-5 for the baud rate codes.

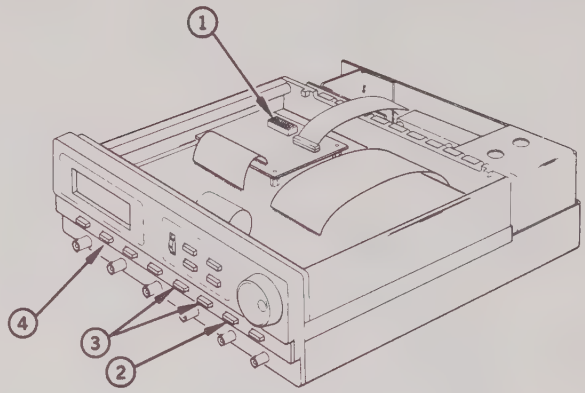


Figure 3-12. RS-232-C Controls and Switches

3.10.2 (Status) Key (2)

Pressing the status button until HAND appears on the display allows the user to examine the handshake mode. Rotating the knob changes the handshake mode between CTS/DTR (hardware handshake) and XON/XOFF (software handshake).

3.10.3 CMD RCL Key (◄►) (3)

For units with any remote option, the ◄ and ► keys are also the CMD RCL (Command Recall) keys. Pressing either one of these keys while in remote displays the last 16 ASCII characters received by the RS-232-C interface. The previously received characters can be scrolled on the display by spinning the control knob. A pointer on the display indicates the position of the viewing window relative to the last received character. Any nonprintable ASCII character except C_R and L_F are displayed as dots. This feature can be used as a debugging tool for remote instrument programming.

3.10.4 GTL (Trigger) Key (4)

If the unit is in remote mode, the Trigger key is actually the GTL (Go To Local) key. Pressing this key brings the Model 23 into local control providing the controller has not locked out the key (see paragraph 3.9).

Table 3-4. Parameter Round Offs

	Round Off Values (Scratchpad Input)		Execute Round Off Values (Scratchpad to Waveform Memory)		
Parameter	**Range***	**Round Off**	**Mode**	**Range**	**Round Off**
Frequency	0.01 Hz to <10 MHz	4 Digits	Synth	0.01 Hz to 12 MHz	No Round Off
	10 MHz to <16 MHz	5 Digits	Clock	0.01 Hz to 32 MHz	No Round Off
	16 MHz to 32 MHz	5 Digits (Up to Next Even LSD)	All Others	0.01 Hz to <10 MHz	3 Digits
				10 MHz to 12 MHz	4 Digits
Amplitude**	10 mVp-p to <10 Vp-p	3 Digits or Nearest 0.1 mVp-p			
	10 Vp-p to 10.2 Vp-p	4 Digits or Nearest 10 mVp-p			
Offset**	−5.1V to +5.1V	3 Digits or Nearest 0.1 mV			
Ampl Vp-p + 2 (Absolute Offset)				10 mVp-p to <0.1 Vp-p	3 Digits or Nearest 0.1 mVp-p
				0.1 Vp-p to <1 Vp-p	3 Digits or Nearest 1 mVp-p
				1 Vp-p to 10.4 Vp-p	Nearest 10 mVp-p
Remaining Parameters		To Closest Integer			None

*Values not shown are invalid.
**Terminated into 50Ω.

Table 3-5. RS-232-C Interface Control Commands

Character	ASCII	Function
!	$21	Causes the Model 23 to go into remote mode. In remote mode the instrument setup can only be changed from the RS-232-C interface and not from the front panel. The front panel keys will still be active and can be used to query the instrument setup conditions. The instrument can be returned back to local mode by sending a '$' over the interface or pressing the Trigger key (unless it is locked out by '*', see below).
$	$24	Causes the Model 23 to return to local mode. In local mode the instrument setup can be changed only from the front panel and will ignore any commands from the interface (except '!').
*	$2A	Causes the Model 23 to disable the GOTO LOCAL (Trigger key). After this, the only way the instrument can return to local mode is with a '$' character from the interface.
?	$3F	Causes the Model 23 to send the talk message as set by the talk mode (XTn) to the connected device.
DC3 (XOFF)	$13	Causes the Model 23 to stop transmitting data to the connected device (see handshaking above).
DC1 (XON)	$11	Cancels the XOFF condition allowing the Model 23 to continue transmitting.

Table 3-6. Programming Reference Guide

Function	ASCII Character	Description
Amplitude	A	An A followed by a number value programs the peak to peak amplitude into the correct impedance at the Func Out connector. Valid amplitude values are 10E-2 to 10.2. For rounding off, refer to table 3-4.
Amplitude Zero (SCM)	A0	Zeros or nulls both the output amplitude and offset. Also allows suppressed carrier modulation. Any future offset programming while in SCM is ignored.
Execute	I	An action command that causes all parameters in the scratchpad to be checked for interparameter conflicts. If no error is found, the rounded scratchpad contents are transferred to the waveform memory. An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.
Exponent	E	Designates the numerals immediately preceding "E" to be raised by the *10 power of the following numeral and ± entries. For example, F3E-1 = Frequency 3* 10^{-1} = Frequency 0.3 Hz.

Table 3-6. Programming Reference Guide (Continued)

Function	ASCII Character	Description
Frequency	F	An F followed by a number value programs the generator frequency in hertz. For rounding off, refer to table 3-4. An "E" designates exponent. Valid frequency values are: Clock Mode 10E-2 to 32E6 Cont/Trig/Gate/Synth Mode 10E-2 ... 12E6 Trig Hav/Gate Hav Mode 10E-2 to 999 Sine/Square/Triangle Func 10E-2 to 12E6 Ramp Up/Ramp Dn Func 10E-2 to 999(.9)
Frequency Zero (FM)	F0	Sets the output frequency to the lower end of the selected frequency range (see paragraph 3.3.7.1). This range is determined by programming a frequency within the limits of that range before programming F0.
Function	C	The character C followed by a single digit code between 0 and 5 selects function at the Func Out connector. FUNCTION CODE Sine wave C0 Square wave C1 Triangle wave C2 Ramp Up C3 Ramp Dn C4 DC C5
Mode	B	The character 'B' followed by a single digit code between 0 and 4 selects the operating mode of the instrument. **MODE** **CODE** Continuous B0 Triggered B1 Gated B2 Triggered Haver (F<1E3 not valid for Ramp Up or Ramp Dn) B3 Gated Haver (F<1E3 not valid for Ramp Up or Ramp Dn) B4 Clock (10 mHz to 32 MHz only valid for sync out signals) B5 Synthesized (same as continuous but with increased frequency accuracy B6
Number Character	0-9, ±, .	The numeric characters (0 through 9, E) are used to program new parameter values. Data entry is free format, i.e., fixed point, floating point and exponential notation, or scientific notation. Fixed Point: Decimal remains at far right.

Table 3-6. Programming Reference Guide (Continued)

<table>
<tr><th>Function</th><th>ASCII Character</th><th>Description</th></tr>
<tr><td></td><td></td><td>Floating Point: You program the decimal point. It floats to the left in its designated position as you enter more numerals.

Exponential Notation: A value, then E followed by the exponent of a times ten multiplier. When the value (mantissa) is limited to one digit, exponential notation is called scientific notation.</td></tr>
<tr><td>Offset</td><td>D</td><td>The Character D followed by a number value programs the offset voltage into the correct impedance at the Func Out connector. Valid offset values are −5.1 to +5.1. For rounding off, refer to table 3-4.</td></tr>
<tr><td>Reset</td><td>Z</td><td>An action command that sets the waveform and scratchpad memories to the defined default values. Refer to paragraph 3.2 number 21 for the initial values.</td></tr>
<tr><td>Trigger</td><td></td><td>In remote operation, triggered and gated modes of the generator are initiated by an external signal at the Trig In connecter, or the J and H commands via the GPIB.</td></tr>
<tr><td>Man. Trig. Pressed</td><td>J</td><td>See following Triggering/Gating Chart.</td></tr>
<tr><td>Man. Trig. Released</td><td>H</td><td>See following Triggering/Gating Chart.</td></tr>
<tr><td>Trigger Slope</td><td>Q</td><td>The character 'Q' selects generator triggering or gating on the rising or falling edge of the Trig In (TTL) signal or RS-232-C 'J' (positive slope) or 'H' (negative slope) command. See TRIGGERING/GATING CHART below.

TRIGGERING/GATING CHART
<table><tr><th></th><th>Positive Slope (Rising Edge) Q0</th><th>Negative Slope (Falling Edge) Q1</th></tr><tr><td>J</td><td>Trig: Single Cycle
Gate: Freeruns</td><td>Trig: Reset
Gate: Off</td></tr><tr><td>H</td><td>Trig: Reset
Gate: Off</td><td>Trig: Single Cycle
Gate: Freeruns</td></tr></table></td></tr>
<tr><td>Talk Mode</td><td>XT</td><td>To read a message from the Model 23, send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Mode (XT) setting. The last character of the Model 23's message will be the currently programmed terminator character with the EOI line asserted.

XT followed by a code (0 through 5) selects the kind of message the 23 will send when it is addressed as a talker on the GPIB.</td></tr>
</table>

Table 3-6. Programming Reference Guide (Continued)

Function	ASCII Character	Description
		Code Message XT0 Programming error list. A typical error string is E 1F 2AD. Some error string characteristics are: A. All error strings begin with E B. Most recent error is at the end of the string C. Errors are separated by space D. Class 1 error: A 1 followed by the programming character that caused the error (example 1F) E. Class 2 errors: A 2 followed by the two conflicting parameters F. Error strings can be up to 80 characters in length H. After transfer, the instrument clears the error string. XT1 Poll Byte response: Provides interface and instrument status information according to the set bits. After reading, the poll byte is set to 0. **Poll Byte** 128 Carrier Lost | 64 1 | 32 Framing Error | 16 Ovrun Error | 8 Batt Low | 4 Undef'd | 2 Exec complted | 1 Program Error XT2 **The most recently selected parameter and its value. Example: Freq 1.23E3. If no parameter is selected, the instrument returns NO PARAMETER SELECTED.** XT3 **The entire instrument setup after last execute. Example: F10E3 A5 D0 B0 C0 Q0.** XT4 The entire instrument setup when execute is received; same format as XT3. XT5 Instrument identification: Wavetek Model 23 V(X.Y). X.Y identifies the software version number.
Terminator Select	XV	Designates the end of a character string. Initially the instrument will accept a C_R or L_F and send 'CR' and 'LF' as a terminator (XV0). The terminator character may be changed to any ASCII character except 'DC1' (XON), 'DC3' (XOFF), and any of the interface control characters '!', '*', '$' and '?' by sending XV followed by the decimal value (argument) corresponding to the new terminator. Example: XV13 changes EOS character to carriage return (CR). XV0 as a special case means that the instrument will accept and send 'C_R' or 'L_F' and send 'CR' and 'LF' as a terminator.

3.11 ERRORS

When an illegal value is programmed or interdependent parameter errors are detected, the Model 23 sets the programming error bit in the poll byte indicating an error condition. The controller can then poll the Model 23 and request further information (such as the programming error list) by sending 'XT0?' and reading the error string.

3.11.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the selected parameter. For example, programming an amplitude of 500 volts will cause a parameter error when the next alpha character is programmed. At this time, the Model 23 disregards the new value and retains the previously programmed value in scratchpad memory.

Table 3-7. Class 1 Error Guidelines

This Parameter	Must (After Rounding) Be Within:
Amplitude	$10*10^{-3}$ and 10.2 (Or "0" for SCM)
Offset	−5.1 and +5.1
Frequency	$10*10^{-3}$ and $32.000*10^{6}$ (Or "0" for FM)
Mode	0 and 6
Function	0 and 5
Trigger Slope	0 and 1
SRQ Mode	0 and 255
Talk Message	0 and 5
Terminator	0 and 127

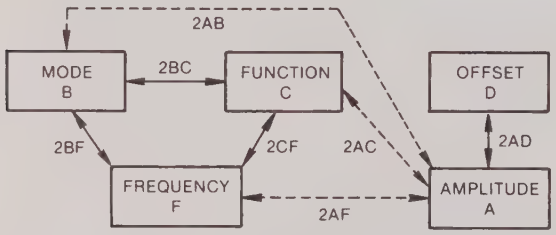


Figure 3-13. Class 2 Errors

3.11.2 Class 2 Errors

Class 2 errors are parameter conflicts or inconsistencies such as 2*ABS (OFST) + peak to peak amplitude greater than 10.4V. Figure 3-13 shows the possible types of class 2 errors. Tests are made every time an execute (I) or GET is given. If no class 2 error is detected, all scratchpad values are transferred to the waveform memory (see table 3-4).

Note that when an Execute (I) or GET is performed, and the programmed frequency value still doesn't satisfy the frequency mode/func relation, an error 2 is detected and none of the scratchpad values are executed.

2AB	A = 0 (SCM) and Mode = Clock	
2AC	A = 0 (SMC) and Function = DC	
2AD	Ampl p-p + 2 * ABS (OFST) > 10.4V	
2AF	A0 and F0 selected (SCM and FM simultaneously)	
2BC	Mode	Function
	Trig Hav (B3)	Ramp Up (C3)
	Gate Hav (B4)	Ramp Dn (C4)
	Trig Hav (B3)	Ramp Dn (C4)
	Gate Hav (B4)	Ramp Up (C3)
	Clock (B5)	DC (C5)
2BF	Mode	Frequency
	Cont (B0)	F > 12.00 MHz
	Trig (B1)	F > 12.00 MHz
	Gate (B2)	F > 12.00 MHz
	Trig Hav (B3)	F > 999 Hz
	Gate Hav (B4)	F > 999 Hz
	Synth (B6)	F > 12.00 MHz
	Clock (B5)	F0 (FM)
	Synth (B6)	F0 (FM)
2CF	Function	Frequency
	Sine (C0)	F > 12.00(0) MHz and not Clock Mode
	Square (C1)	F > 12.00(0) MHz and not Clock Mode
	Triangle (C2)	F > 12.00(0) MHz and not Clock Mode
	Ramp Up (C3)	F ≥ 1 KHz and not Clock Mode
	Ramp Dn (C4)	F ≥ 1 KHz and not Clock Mode
	DC (C5)	F0 (FM)

SECTION 4
CIRCUIT DESCRIPTION

4.1 MODEL 23 GENERAL DESCRIPTION

Figure 4-1 shows a simplified block diagram of the entire Model 23 Synthesized Function Generator. The microprocessor section, which receives instructions from the operator interface (keyboard and control knob) or remote interface (options 001 or 002), controls all operations of the instrument. These instructions direct the microprocessor to send control signals to the appropriate waveform generation circuits (frequency synthesizer, function generator and waveform synthesizer) and the output block. Instrument parameters are continuously maintained in microprocessor memory through the use of a battery located in the battery test portion of the microprocessor circuitry, allowing the instrument to power-up under the same parameters that existed when the instrument was last powered-down. The microprocessor converts frequency and amplitude parameters to the proper units and sends all instrument set-up parameters to the front panel display.

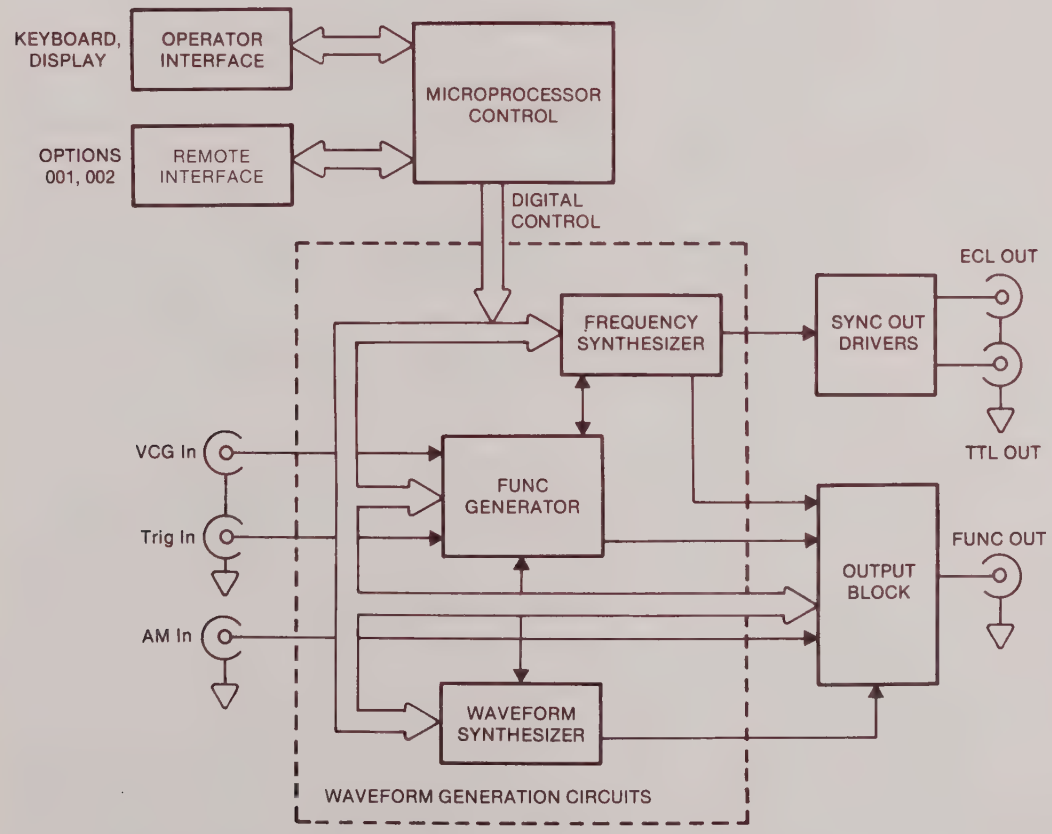


Figure 4-1. Model 23 Complete Block Diagram

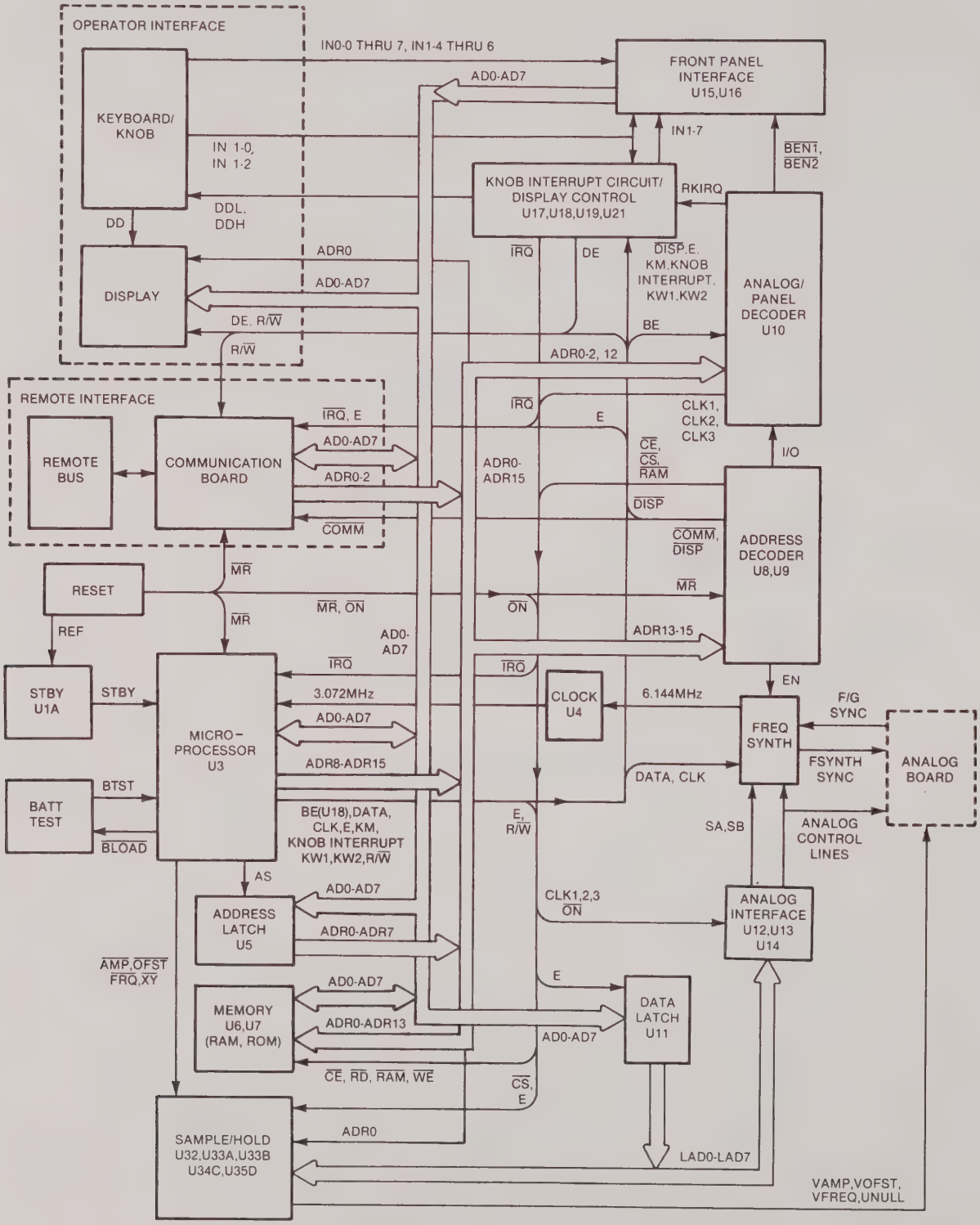


Figure 4-2 Microprocessor Control

The remote interface located on the communication board (options 001 or 002) interfaces with the instrument's microprocessor and handles all the handshake protocol and data transfer over the remote bus. The microprocessor insures that the remote interface overrides any front panel keyboard commands.

Within the frequency range of 1 kHz to 12 MHz, the function generator section produces sine, triangle and square waveforms in continuous, triggered, gated or synthesized modes. The VCG In connector provides for an external voltage input to control the function generator frequency in sweep or FM operation. The microprocessor disables this connector in frequency synthesized mode.

In triggered mode, each time the trigger logic circuit (within the function generator) is clocked, a single waveform cycle is produced by the function generator. In gated mode, the function generator produces a continuous output waveform as long as the trigger is enabled, completing the last cycle begun. The trigger logic circuit is clocked from the front panel Trigger switch, an external signal at the Trig In (TTL) connector or a remote interface command.

When the synthesizer mode is selected, a very accurate and stable square wave frequency reference from the frequency synthesizer (located on the microprocessor/synthesizer board) is used to maintain the function generator frequency within very tight tolerances.

From 10 mHz to 1 kHz, the function generator loop clocks the digital waveform synthesizer, providing sine, triangle, and square waveforms, up or down ramps, and triggered or gated haverwaves. The function generator drives a $\div 1/\div 100$ circuit, the output of which clocks the waveform synthesizer producing 1 cycle for every 1000 or 100,000 cycles from the clock input.

The output block selects the appropriate waveform to be output, allows for Amplitude Modulation (AM) and Suppressed Carrier Modulation (SCM) by utilizing the AM In connector, then provides the final gain and output offset requirements for the selected waveform before reaching the Func Out connector, which is operational to 12 MHz.

ECL and TTL level square waves from the ECL Out and TTL Out connectors are available from 10 mHz to 32 MHz. The frequency synthesizer selects one of three signals to drive the ECL and TTL outputs. These signals originate from the waveform synthesizer for frequencies between 10 mHz and less than 1 kHz, the function generator from 1 kHz to 12 MHz, and the frequency synthesizer from greater than 12 MHz to 32 MHz (CLOCK mode only).

4.2 DIGITAL CONTROL DETAILED CIRCUIT DESCRIPTION

4.2.1 Microprocessor Control

The following descriptions refer to the figures specified and the microprocessor/synthesizer schematics in the back of this manual. Figure 4-2 shows a block diagram of the microprocessor control circuitry. The heart of this section and clearinghouse for all control operations is the 6303 microprocessor (U3). It accepts commands from the front panel keyboard through the front panel interface (U15, U16), or the remote interface (option 001 or 002) through the communication board. The software program located in external Read Only Memory (ROM, U6) provides information needed to do the various routines. The ROM is addressed by port 3 (AD0-AD7) and port 4 (ADR8-ADR15). As operating parameters are updated, they are stored in Random Access Memory (RAM U7) and sent to the front panel display. The data latch (U11) reads these updated parameters and stores them for use by the analog interface (U12, U13, U14) and sample and hold circuit (U32). The output of the analog interface controls the waveform generation circuits at the analog board and the frequency synthesizer. The knob interrupt circuit (U17, U18) reads data from the front panel knob (IN1-0, IN1-2) and the microprocessor (U3) to interpret the direction and speed of knob rotation. The analog/panel decoder enables the analog interface, front panel interface and knob interrupt circuits. Additionally, microprocessor port 1 (see P10-P17, schematic 0103-00-1454, sheet 1 of 2) controls the frequency synthesizer, digital to analog converter, and knob interrupt circuits, while port 2 (P20-P24) controls the battery test and knob interrupt circuits.

Figure 4-3 shows the approximate timing for major signals and busses in the microprocessor system. Actual system timing varies somewhat from instrument to instrument, so signal spacing may be different within the period of the system clock.

The multiplexed low-order address/data bus AD0-AD7, provides both address and data information. The address is valid during the low part of the E clock cycle while the Address Strobe (AS) is high. The falling edge of AS latches the address. Data is placed on the same lines during the second half cycle while the E clock is high and remains valid until 20 ns after the falling edge of the E clock.

The microprocessor responds to two interrupt inputs. Master reset ($\overline{\text{RESET}}$) initializes the microprocessor, while the external interrupt request line ($\overline{\text{IRQ}}$) from the knob interrupt or communication board signals the processor of an interrupt condition.

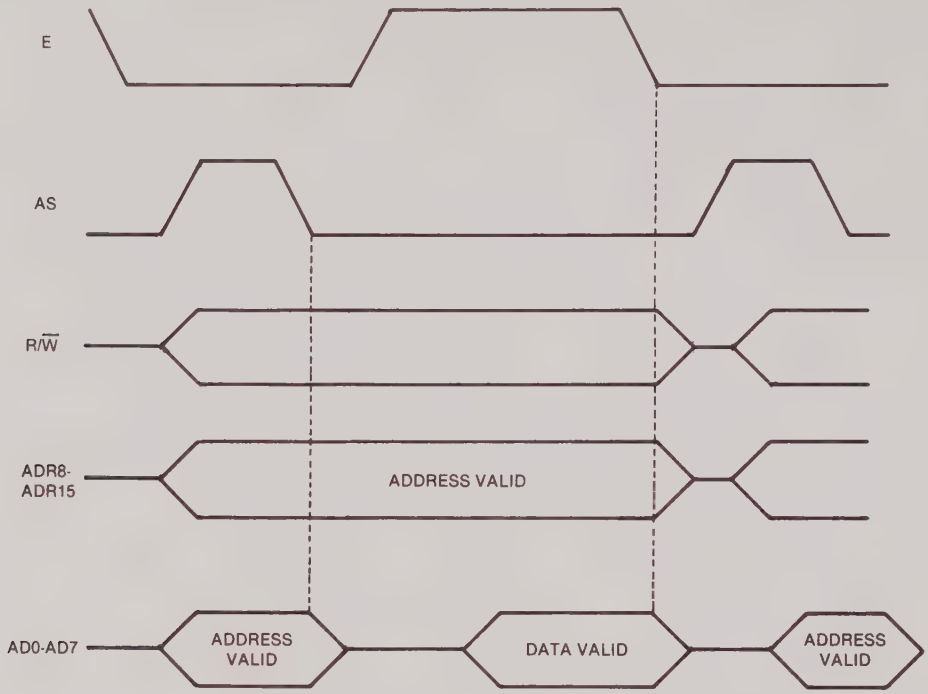


Figure 4-3. Multiplexed Bus Timing

Sleep: If no setting changes are given to the processor from the front panel or the communication board the processor enters sleep mode. During sleep, the ports and busses are in a quiescent state. This results in a lower power consumption and a lower noise level.

Pin Conditions During Sleep

Power Supplies	Remain Active
Clock Input	Remains Active
Reset	Remains Active
STBY	Remains Active
IRQ	Remains Active
NMI	Remains Active
E clock	Remains Active
AS	Remains Active
I/O Ports	Retain condition before sleep
A8-A16	Output "1"
AD0-AD7	If E low; Output "1"
	If E high; High impedance
R/W	Output "1"

The processor exits sleep mode if an internal or external interrupt is received. External interrupts come from the front panel or communication board. Internal interrupts occur ≅ every 30 ms. The sample and hold settings are refreshed at each internal interrupt.

4.2.2 Microprocessor Clock

The microprocessor receives its clock signal from the frequency synthesizer, U22 (0103-00-1454 Sheet 2 of 2). The 6.144 MHz) signal at U22 pin 15 is divided by 2 at U4 (sheet 1) and applied to the microprocessor, U3 pin 3. Signal routing is via coax cables.

4.2.3 Front Panel Interface

The front panel interface inputs user programming information from the front panel. The microprocessor enables the interface via the analog/panel decoder at ≅ 30 ms intervals. The panel data is then placed on the data bus. When the interface is not enabled, the panel data lines are tri-stated. If a knob interrupt is generated, U16 of the front panel interface is enabled and reads the data lines to determine the direction and speed of knob rotation.

4.2.4 Address Latch

The address latch, U5, retains the lower order address bits (AD0 through AD7) from the microprocessor. These bits are latched by AS (U3 pin 39) while the E clock is high and remain valid until 20 ns after the falling edge of the E clock.

4.2.5 ROM

The ROM (read-only-memory), U6, contains the program for the microprocessor. $\overline{CE}$ from the address decoder enables the IC on the rising edge of E clock. Read and write cycles are accomplished by gating the E clock with R/$\overline{W}$ to produce $\overline{RD}$ (Read Enable) and $\overline{WE}$ (Write Enable).

4.2.6 RAM

The microprocessor uses U7 as a scratch pad memory. The RAM address lines (A0 through A10) select a location for storage or retrieval of digital data. The location corresponds to the binary value of the logic levels on the address lines. The $\overline{RAM}$ line from the address decoder enables the RAM on the rising edge of the E clock. During a write cycle, the write pulse circuit NANDs the read/write line from the processor (R/$\overline{W}$) with the E clock to generate a write pulse (U7 pin 21) after all address lines have become stable. A lithium battery (BT1) maintains a sufficient voltage level to prevent the loss of information stored in RAM when external power is removed.

The RAM data ports are bi-directional. The RAM places data on the lines when the OUTPUT ENABLE ($\overline{OE}$) port is pulled low by the $\overline{RD}$ line. To read data into the RAM, the RAM output is disabled by a high on the $\overline{RD}$ line.

4.2.7 Data Latch

The data latch (U11) demultiplexes and holds information from the multiplexed bus for transfer to the analog interface and sample and hold circuits. This data is transferred on the negative transition of the E clock.

4.2.8 Analog Interface

The analog interface consists of three octal type "D" flip-flops (U12, U13 and U14) that are used as data registers to latch digital information from the data latch bus (LAD0 through LAD7) for use by the waveform generator board and frequency synthesizer. Each register is clocked on the rising edge of the clock pulse from the analog/panel decoder (CLK 1, CLK 2 and CLK 3) when the data on the data latch bus is valid for that particular register.

4.2.9 Knob Interrupt

Pins 1 and 2 of J12 transfer data (CPRE1 and CPRE2), which when interpreted, describe front panel knob rotation. This data originates from the CPRE (Conductive Plastic Rotary Encoder) shown in figure 4-4. When the front panel knob is turned, the two concentric rings remain stationary while both pick-off points at the top of the diagram spin together as a unit on the bearing (center). Mounted on each ring are 50 contact points which are displaced by 25% between rings. Figure 4-5 shows the 25% displacement of the contact points on the two rings as if the rings were cut and laid flat. As the knob is spun and the contact points on each ring reach the appropriate pick-off point, the attached CPRE line is shorted through 30KΩ to ground, producing pulse trains which are transferred through CPRE1 and CPRE2

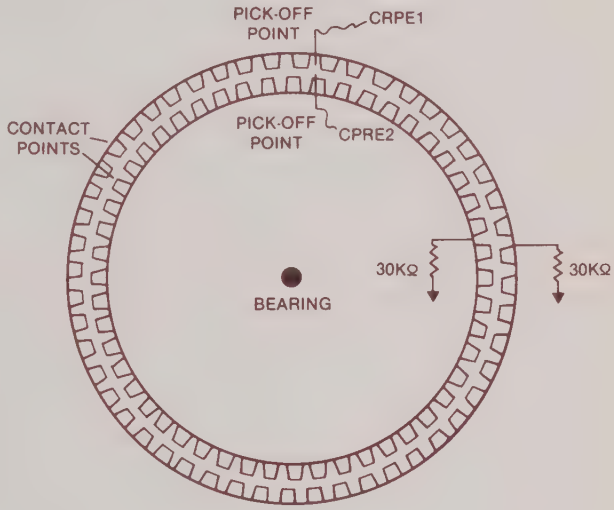


Figure 4-4. Conductive Plastic Rotary Encoder

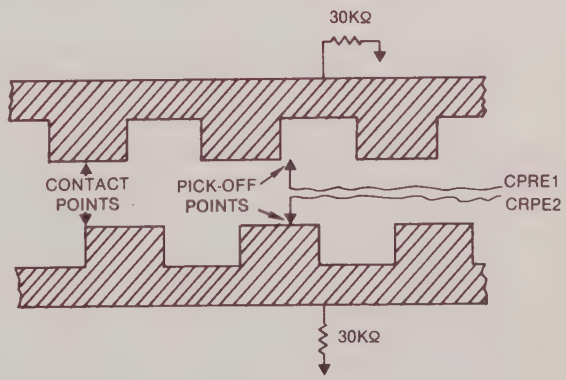


Figure 4-5. Contact Point Relationship

to the knob interrupt circuit. Because of the 25% contact point displacement between rings, points on the two pulse trains are displaced by 90° and the lead or lag of the displacement indicates direction of rotation as described in the following paragraph.

The microprocessor prepares to read a transition of one of the CPRE lines (CPRE1 or CPRE2) by setting RKIRQ high and placing the compliment of CPRE1 at KW1 (P20 on the microprocessor), and CPRE2 at KW2 (P22 on the microprocessor). For this example, suppose CPRE1 is high (making KW1 low) and CPRE2 is low (making KW2 high). Since the inputs of both exclusive-or gates (U18) are complimentary, their outputs are high. The microprocessor also sets KM (P17 on the microprocessor) to be the opposite of its last state, and for sake of this discussion, KM is high. With KM high, U17 pin 5 is low, and pin 6 will be high, preventing CPRE1 from having any effect on the circuit. Because U17 pins 9, 10 and 11 are all high, pin 8 is low. U19 pin 11 is high, knob interrupt (P12 on the microprocessor) is low and $\overline{IRQ}$ is high. This condition will remain in effect until CPRE2 makes a transition, which in this example would be low to high. When this occurs, U18 pin 6 will go low and U17 pin 8 will toggle high, putting a low at U17 pin 12, a high at knob interrupt, and a low at $\overline{IRQ}$, interrupting the microprocessor. Because the interrupt could have come from either the CPRE or the communication board, the microprocessor must interrogate the knob interrupt line to locate the interrupt source. Finding knob interrupt high, it then reads the conditions of CPRE1 and CPRE2, loading the compliment of CPRE1 in KW1 and the compliment of CPRE2 in KW2. It also inverts KM, and calculates the direction of knob direction. In this example, KM was high, KW2 was high, and CPRE1 went high when the knob was turned. From table 4-1 we find that the knob was rotated counterclockwise. Having completed the knob interrogation, the microprocessor pulls RKIRQ low for ½ a clock cycle, forcing U17 pin 12 and $\overline{IRQ}$ high. With U17 pins 3, 4 and 5 all high, pin 6 goes low. CPRE2 is now disabled and KM goes low, leaving only a logic level change at CPRE1 to affect the circuit. Table 4-1 shows the 8 possible conditions that determine direction of knob rotation.

Since each ring produces 50 pulses per rotation, and an interrupt is generated at each pulse edge, two hundred interrupts are generated per knob rotation, or one interrupt approximately every 700μs if the knob is spun at 7 revolutions per second.

4.2.10 Analog/Panel Decoder

The analog/panel decoder (U10) determines which interface (analog interface, front panel interface, or knob interrupt circuit) will latch data into its registers at any given time. The decoder is enabled by a "1" on ADR12, a "0" on I/O and the high portion of the E clock cycle. The binary value of ADR0, ADR1 and ADR2 selects the appropriate interface. For example, an address of "000" selects output Y0 (CLK1 enabling U12), while address "111" selects output "Y7" (RKIRQ enabling U17). CLK 1, CLK2 and CLK3 are clock lines for the analog interface (U12, U13 and U14), $\overline{BEN1}$ and $\overline{BEN2}$ are enable lines for the front panel interface buffers (U15 and U16) and RKIRQ is an active low control line for the knob interrupt circuitry.

4.2.11 Address Decoder

The address decoder, U8/U9, decodes the upper 3 bits (ADR13, ADR14 and ADR15) of the 16 address lines to

Table 4-1. Direction of Knob Rotation

Before Interrupt			During Interrupt		Direction of Knob Rotation
KM	KW1	KW2	CPRE1	CPRE2	
Low	Low	—	—	Low	CW
Low	Low	—	—	High	CCW
Low	High	—	—	Low	CCW
Low	High	—	—	High	CW
High	—	Low	Low	—	CCW
High	—	Low	High	—	CW
High	—	High	Low	—	CW
High	—	High	High	—	CCW

Table 4-2. Address Decoder Memory Locations

ADR13	ADR14	ADR15	Select	Function
1	1	0 or 1	$\overline{CE}$	Selects EPROM in the range of C000 to FFFF
1	0	1	EN	Enables data transfer to PLL chip in the frequency synthesizer
1	0	0	$\overline{CS}$	Selects DAC IC U32
0	1	1	$\overline{RAM}$	Selects RAM IC U7
0	1	0	$\overline{COMM}$	Selects communication interface board
0	0	1	$\overline{DISP}$	Enables the Display
0	0	0	I/O	Enables the analog/PLL Interface

select one of eight possible addressable devices or circuits. These are the ROM ($\overline{CE}$), the frequency synthesizer (EN), the sample and hold ($\overline{CS}$), the RAM ($\overline{RAM}$), the communication board ($\overline{COMM}$), the display ($\overline{DISP}$) and the analog/panel decoder ($\overline{I/O}$). Table 4-2 shows the address for each of the these blocks.

4.2.12 Sample and Hold

A sample-and-hold section provides four analog voltages (VAMP, VOFST, VFREQ and VNULL) that control the function generator. This section consists of the DAC (digital-to-analog converter) (U32), the −10.24V reference for the DAC (U33A), and four sample-and-hold circuits (U35) that demultiplex the DAC output to provide four separate analog control voltages for the waveform generator board.

4.2.12.1 Digital-to-Analog Converter (DAC)

The 10-bit digital-to-analog converter, U32, which interfaces directly to the latched data bus (LAD0-LAD7), contains its own internal data latching registers. When the microprocessor transfers data into the DAC with $\overline{CS}$ low and ADR0 high, the negative transition of $\overline{WR}$ and $\overline{XFER}$ latches the most significant 8 bits from the data lines into the DAC's internal register. A second transition of $\overline{WR}$ and $\overline{XFER}$ with both $\overline{CS}$ and ADR0 low latches the least significant bits. The current output of the DAC (U32 pin 12) is converted to a voltage output by operational amplifier U33B at pin 1 using feedback internal to the DAC at U32 pin 14.

4.2.12.2 DAC Voltage Reference

Since the DAC circuit provides an inverted programmable portion of the reference voltage, the reference must be negative to get a positive output. This negative voltage is generated by operational amplifier U33A with a gain of −0.681. It uses the regulated +15V power supply as its input. The reference voltage provides approximately a 10 mV step for each binary step of the DAC.

4.2.12.3 Sample and Hold

The microprocessor sequences the DAC through four discrete voltages at about 1 ms each (4 ms for a complete cycle). The four sample-and-hold circuits latch each of these analog voltages in turn to provide the four separate analog control voltages to the function generator board appearing at J6. In the following paragraph, component designations refer to the sample and hold circuit that generates VAMP which controls the amplitude on the waveform generator board. The other sample and hold circuits act similarly.

Within a few microseconds after the appropriate voltage appears at the output of the DAC circuit, the sample-and-hold control line ($\overline{AMP}$) from the microprocessor U3 pin 16 goes low and turns on the analog switch U34A. The DAC output charges the holding capacitor C79 until the control signal from the microprocessor U3 pin 16 turns analog switch U34A off in order to load U34B with its information. The analog switch's high output impedance in the "off" state and the high input impedance of the

buffer at U35A maintain the voltage on the output of the circuit with negligible discharge until the next cycle selects this sample-and-hold circuit again. R61 and C80 constitute a high frequency filter.

The control lines for the four DAC circuits are: $\overline{AMP}$ (P13 on microprocessor), which controls amplitude; $\overline{OFST}$ (P14 on microprocessor) which controls offset; $\overline{FRQ}$ (P15 on microprocessor) which controls frequency; and $\overline{XY}$ (P14 on microprocessor) which controls the VNULL input to the XY multiplier. When one of these control lines goes low, the appropriate analog circuit is driven by the DAC.

DAC Programming

Signal	Function	Source
ADR0	Controls byte sequencing	Address Latch
$\overline{CS}$	DAC Chip Select	Address Decoder
$\overline{WR}$	Write to Latch	Inverted E Clock
$\overline{XFER}$	Used with "Write to Latch" to transfer data to Dac Register	Inverted E Clock

4.2.13 Reset

During initial power up, the clock generator is unstable for several cycles causing the internal state and I/O ports to be random. To prevent writing erroneous data into from RAM during this time, U7 is disabled. At power on, MR (pin 6 on the microprocessor) is low for a minimum of 20 ms as C2 charges. With $\overline{MR}$ low, the switches in U9 (pins 1, 2, 10 and 11) are open, and R18 forces $\overline{RAM}$ high, disabling U7. When C2 has charged to a predetermined level, $\overline{MR}$ goes high, the switches in U9 close, and U8 pin 12 is allowed to control $\overline{RAM}$/.

Pressing the RESET button directs the software to reinitialize all operating parameters to a predetermined setting. The reset circuit (U2) is not used during this operation.

4.2.14 Standby

To prevent excessive battery drain as the instrument is powered down, U3 pin 7 ($\overline{STBY}$) goes low to disable the microprocessor. However, in order for the microprocessor to stabilize during power up, $\overline{STBY}$ must go high at least 20ms before $\overline{MR}$ goes high. At power up, the + 5V supply pulls U1A pin 3 to about 2.7V, while pin 2 is held at about 2.5V by the reference circuit in U2 pin 1. This causes U1A pin 1 to go high, enabling the microprocessor at $\overline{STBY}$. When the instrument is powered down, the voltage at U1A pin 3 drops below the reference voltage at pin 2, causing the output at U1A pin 1 to go low, shutting down the microprocessor.

4.2.15 Battery Backup/Test:

To maintain the last instrument set-up after power is removed, the supply voltage for the microprocessor (U3 pin 21), RAM (U7 pin 24) and RAM select switch (U9 pin 14) are backed up by a non-rechargeable 3V lithium battery (BT1) which holds BBV (Battery Backup Voltage) to about 2.8V. During the time that the instrument is operating, power is provided by the instrument's + 5V supply. About 200mV is dropped across CR2, leaving about 4.8V for BBV. CR3 is reversed biased, blocking current between the supply voltage and BT1.

When instrument line power is removed, the + 5V supply falls below the 3V battery voltage which, through diode CR3, begins to supply the voltage necessary for data retention. Diode CR2 is reversed biased and prevents the battery from discharging through the rest of the circuit.

The battery test, performed during either a power up or status check, insures that the battery is sufficiently charged. During this test, the microprocessor loads the battery by pulling $\overline{BLOAD}$ (P23 on the microprocessor) low which draws between 70 and 100 μA of current from the battery. If the battery voltage drops below 2.16V, the microprocessor will cause the display to read "BATTERY LOW!".

4.3 OPERATOR INTERFACE

The operator interface consists of the front panel keyboard, knob assembly, display and display angle adjustment.

4.3.1 Keyboard

When a front panel key is pressed, the closed contact shorts that control line (which is input to the front panel interface) to ground. When the microprocessor causes the front panel interface to be strobed by the analog/panel decoder, the logic level of the microprocessor control lines (AD0 through AD7) instruct the microprocessor to call the appropriate routine for the key pressed.

4.3.2 Knob

Effectively, the knob consists of two rotary switches with no starting or ending points. See paragraph 4.2.9 for a description of the knob and how it interfaces with the knob interrupt circuit.

4.3.3 Display

The DISPLAY connector J10, links the 16 character × 2 line display with the microprocessor. When $\overline{DISP}$ is brought low by the address decoder, the display is enabled through DE with each positive transition of the E clock. Being an intelligent device, the display is able to receive and decode programming instructions (ADR0 low) and data (ADR0 high) from the 8 bit data bus (AD0 through AD7).

4.3.4 Display Angle Adjustment

The display angle adjustment is a vernier that allows the user to adjust the viewing angle of the LCD to optimize display legibility. The vernier end terminals are connected through resistors on the microprocessor/synthesizer board to the + 5V and − 15V supplies. The wiper (DD), which has a voltage swing of + 2V to − 2.5V is connected to the display by way of the microprocessor/synthesizer board.

4.4 REMOTE INTERFACE (OPTION 001 OR 002)

The remote interface option allows the Model 23 to be controlled from an external source such as a computer or controller. Two interfaces are available, IEEE-488 (GPIB) and RS-232-C.

4.4.1 IEEE-488 Interface (Option 001)

The IEEE-488 interface is located on the communication board mounted on the microprocessor/synthesizer board. Most of the IEEE-488 instrument bus protocol functions are handled by the General Purpose Interface Adapter (GPIA), a single IC, U2. Data and control portions of the bus require high current driving capability and specific line termination which the Bus Drivers, U3 and U4, provide. These two sections of the bus have different requirements depending on whether the instrument is acting as a talker or a listener: the data transceiver, U3, always acts as a transmitter during talk modes and a receiver during listen modes, but the control transceiver requires that some lines transmit while others receive in both of these modes. These different requirements are met by using different parts for each function (the 75160A for data and the 75161A for control).

The IEEE-488 Interface IC, U2, meets all the handshaking requirements of the 1978 IEEE-488 standard. When there is a pending interrupt, $\overline{IRQ}$ (U2 pin 40) is asserted low. This alerts the microprocessor of an interrupt condition, causing it to interrogate the eight registers internal to U2. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data registers in U2; data output (talk mode) is written to the same register location.

4.4.1.1 GPIB Address

A 5 section DIP switch (SW1), selects the GPIB address for the instrument. Only binary 0-30 are valid settings. The address strobe enable line ($\overline{ASE}$) from the interface IC, U2, controls the select line to U1 that enables the address switch, SW1. The microprocessor can read this switch by reading the address register in U2, which causes U2 to set $\overline{ASE}$ low during the E-clock (data) portion of the microprocessor clock cycle. This address is not necessarily the address used by the interface IC (U2); that address is stored in U2 by writing into the internal address register. The actual address of the instrument can be changed by front panel control, but will return to the address specified by the address switch during a microprocessor reset cycle (power-up).

4.4.2 RS-232-C Interface (Option 002)

The RS-232-C interface is located on the communication board mounted on the microprocessor/synthesizer board. Most of the instrument bus protocol functions are handled by the Asynchronous Communications Interface Adapter (ACIA), a single IC, U1. CS0 and CS1 (chip select) are both held high so that when $\overline{COMM}$ pulls CS2 low, U1 is enabled to either read or write on the data bus (AD0 through AD7). The RXD input line is used to enter the serial data. The $\overline{RTS}$ handshake line is asserted if the microprocessor's internal data buffer is full. This prevents further data transmissions until the data in the buffer is processed. The TXD output is used to transmit the serial data when the CTS line is low.

When R/$\overline{W}$ (Read/$\overline{Write}$) is low, the ACIA receives data from microprocessor, but when high sends data to microprocessor. The Register Select (RS) line selects the transmit/receive registers in ACIA when high, and the control/status registers when low. The E Signal from microprocessor enables the bus input and output data buffers within the ACIA. Logic gates, U3 and U4, provide signal conditioning between the bus and the ACIA. The transmit (TXCLK) and receive (RXCLK) clock inputs are connected together and originate from the Z output of bit rate generator U2. Transmit is enabled on the negative transition and receive is enabled on the positive transition. A crystal oscillator circuit consisting of Y1, R1, C1 and C2 drives U2. Because of the difference in baud rate of various equipment, the baud rate at the Z output is selectable through bit switch SW1 as shown in section 2.

4.5 FUNCTION GENERATOR GENERAL DESCRIPTION

The function generator is a continuous loop which produces simultaneous triangle and square waveforms from 1 kHz to 12 MHz. Figure 4-6 shows the generator loop (bold arrows) and associated circuitry that will be discussed here.

The VCG circuit (ref: schematic 0103-00-1455 sheet 1) produces two adjustable constant currents, I Source and I Sink, determined by the frequency control voltage (VFREQ) from the sample and hold section of the microprocessor/synthesizer board. These currents are alternately selected by the current switch to linearly charge or discharge one of four sets of range capacitors located in the frequency range switches circuit, producing a triangular waveform. The generator frequency is determined by the magnitude of the I Source and I Sink currents and the value of the selected timing capacitor which they charge and discharge. The triangle buffer drives the comparator which compares each triangle peak against a reference voltage called the comparator threshold level, determined by the +COMP and −COMP currents from the high frequency compensation circuit. When the triangle reaches this level, the comparator switches output states, producing the square waveform. The high frequency compensation circuit proportionately decreases the comparator threshold level to compensate for time delays inherent in the loop at high frequencies. The state of the comparator output

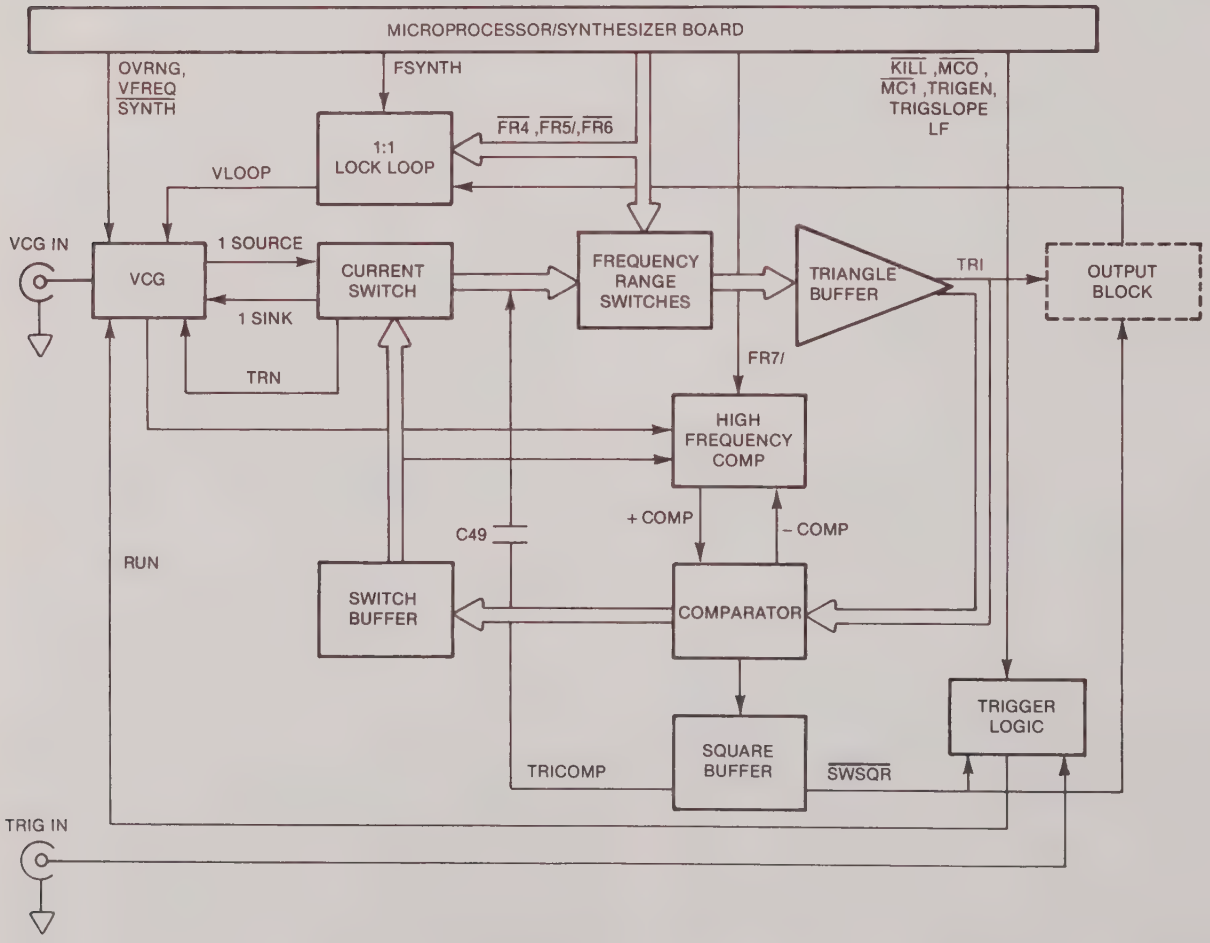


Figure 4-6. Function Generator Loop

determines the polarity of the switch buffer and therefore the polarity of the current switch and direction of charge/discharge current through the selected range capacitor. A second comparator output drives the square buffer which controls the trigger timing in the mode logic, drives the square selector, and is directed to the frequency synthesizer (microprocessor/synthesizer board) for possible use as the driver for the TTL and ECL outputs. Comparator outputs to the switch buffer and square buffer are 180 ° out of phase.

The trigger logic circuit provides the instrument with trigger and gate capabilities. This circuit is digitally controlled by logic signals MC0, MC1 and Trig Slope from the microprocessor/synthesizer board. The Trig In connector provides external trigger and gate capabilities.

When the instrument is in synthesized mode, the 1:1 lock loop circuit compares square waves from the frequency synthesizer and square selector (in the output block circuitry) to produce an instantaneous voltage at VLOOP which corrects the loop frequency.

4.6 WAVEFORM GENERATOR DETAILED DESCRIPTION

4.6.1 VCG

The VCG amplifier (U23) converts control voltages from the VCG In connector (external control), VFREQ (front panel knob) and VLOOP (synthesized mode) into positive and negative currents that control the current source and sink circuits (U25) to set the desired frequency within the selected frequency range. $\overline{\text{OVRNG}}$ provides an extra 0.2mA to push the top range from 10MHz to 12MHz.

The input stage acts as a summing amplifier. The control voltage from the microprocessor/synthesizer board, VFREQ develops a current through R83 and R84 into the summing node, pin 6 of U23. R83 and R84, with C66, also act as a filter for the VFREQ line to reduce the sample and hold switching noise. Any input voltage at the external VCG In connector contributes to the first stage output. CR29 and CR30 prevent excessive voltage at VCG IN from damaging the VCG amplifier. For frequencies between 10MHz and 12MHz, an overrange control, $\overline{\text{OVRNG}}$, adds a fixed 0.2mA through R82 to increase the maximum voltage out of the first stage (or current out of the entire VCG circuit). A gain adjustment (R86) in the first stage is used to control the top-of-range frequency. R96 controls the first stage offset to zero the low end of the external VCG input. The output of the VCG amplifier, U23 pin 7, drives the variable current source and sink as well as the high-frequency compensation circuit.

The current sources operate on the following principles:

1. The collector current of a transistor depends on its base current and current gain. It is relatively independent of collector load resistance.
2. The base drive of a transistor can be adjusted to provide a known reference current through a known collector resistance.
3. This same base drive, applied to a second matched transistor, will cause the second transistor to have the same collector current as the first transistor.

The voltage at U23 pin 7, which is negative in proportion to the sum of all frequency inputs, is reduced by voltage divider R81 and R75, then applied to U23 pin 2. The difference between the voltage at U23 pin 1 and the − 15V supply, minus the voltage from U25 pin 1 to pin 2, divided by the 1KΩ emitter resistor U27 pins 1 to 16 determines the amount of current flowing through current sink transistor U25 pin 3. When this collector current is correct, the voltage at resistor U27 pin 15, and therefore U23 pin 3 is equal to the voltage at U23 pin 2, maintaining the input voltages of U23 pins 2 and 3 equal at equilibrium. The current in U25 pin 3 is duplicated in pins 6, 9 and the collector of Q21. U25 pin 6 provides I sink to the generator loop.

The current source operates in a similar manner, and tracks the current sink. Operational amplifier U23 pin 8 drives transistor U25 pin 15 to whatever value collector current is required to maintain a "virtual ground" at the junction of R27 pins 2 and 4. Since these two resistors are in series, their currents are equal ($I\ Source_{ref} = I\ Sink_{ref}$). The U25 pin 14 base drive is also applied to matched transistor U25 pins 10, 11 and 12 to generate the positive current source (I Source) for the generator loop.

The current sink circuit also generates a current which is used to clamp the triangle node (TRN) at ground potential during the "off" state in the triggered and gated modes. The same transistor base drive that creates the negative current source (I Sink) is also applied to transistors U25 pin 8 and Q1, driving each transistor to a collector current equal to I Sink. The two collectors are connected in parallel to provide a current equal to twice the I Sink current source. This − 2I current is supplied through CR26 by the trigger circuit while the generator is gated "on" (RUN is high).

When the generator is gated "off", a negative voltage is applied to the CR26 anode. This transition always occurs at the negative peak of the triangle waveform, and the − 2I current is momentarily supplied by U22 pin 3. As the triangle node rises toward ground potential, a greater proportion of the − 2I current flows through U22 pin 1. Equilibrium is reached when the trigger holding

current is equal to the positive current (I Source) being supplied to the generator loop, and the triangle node voltage cannot rise any further. Since the matched diodes (U22) have equal currents through them and U22 pin 4 is grounded, the voltage drops across the two diodes will also be equal and the triangle node will be held at ground potential. This stops the waveform as the rising edge of the triangle reaches 0V and ensures that at least one complete cycle will be generated every time the generator is triggered.

R88 adjusts the current source to precisely match the current sink and therefore maintain waveform symmetry. R70, which adjusts the low end frequency, sets the offset of the positive current amplifier, U23 pin 10, to match the offset of the negative current amplifier, U23 pin 3. R73 adds or subtracts current through the reference string to balance symmetry at low currents. The 8.2V zener diodes, CR24 and CR25, allow U25 pins 14 and 1 to approach the positive and negative supply rails respectively. Diodes CR23 and CR44 prevent latch-up in case the VCG circuit is overdriven by the sum of its inputs.

4.6.2 Current Switch

The current switch (ref: schematic 0103-00-1455 sheet 2) which consists of the diode switches (CR10, 11, 12, 13), current source buffer (Q5) and current sink buffer (Q4) has three inputs and one output. The inputs are the positive and negative currents (buffered by Q4 and Q5) and the control voltage from the switch buffer. The output is the switched current that alternately allows the charging (I Source), and discharging (I Sink) of the selected frequency range capacitor (see Frequency Range Switches) to produce a triangle waveform.

The current switch sources current buffered by Q5 (I Source), or sinks current buffered by Q4 (I Sink) at the switch output (junction of CR12 and CR13). The instantaneous polarity of the Switch Buffer output control line (junction of R33 and R34) determines the direction of current flow.

With the control line positive (+ 2V), CR11 and CR12 are reverse biased and I Source current through CR13 linearly charges the selected timing capacitor. At the same time, current flows from the control line through CR10 into the current sink. With the control line negative (− 2V), CR10 and CR13 are reverse biased. The timing capacitor linearly discharges through CR12 to the current sink and current is sourced through CR11 into the control line.

4.6.3 Frequency Range Switches

The frequency range switches (ref: schematic 0103-00-1455 sheet 2) consist of the three basic range capacitors and their controls. Each range capacitor or set of capacitors normally covers 10% to 100% of full scale of its related decade frequency range. As the frequency is changed, a logic level signal from the analog interface (Microprocessor/Synthesizer Board) automatically steps the ranges up or down. For example, when $\overline{FR6}$ goes low, it turns on Q1 which sources about 30 mA through R11 and diodes CR5 and CR8. With CR8 forward biased, the diode's impedance to ground is less than 2Ω and the range capacitor set (C26, C29 and C38) is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, Q1 is turned off and R9 pulls the anode of CR5 to − 15V. The voltage divider, R4 and R8, brings the anode of CR8 to − 7.5V through the 10 MΩ resistor R5, reverse-biasing CR8. This provides a very high impedance, disconnecting the range capacitor. Frequency range control lines ($\overline{FR4}$ and $\overline{FR5}$) operate in the same way connecting selected capacitors C27 (0.1 μF) and C28 (0.01 μF) to the TRN line.

Capacitance for the highest frequency range consists of all the stray capacitance at the triangle node added to C25 and C37 (the 1 MHz bottom of range adjustment capacitor).

4.6.4 Triangle Buffer

The triangle buffer (ref: schematic 0103-00-1455 sheet 2) consisting of Q6, Q7, Q9 and associated components, is a high speed, high impedance input FET voltage follower with a low impedance emitter follower output and unity gain. It buffers the current switch and selected frequency range capacitor from low input impedance circuits in the output block and the comparator. The difference between the input and output voltages is controlled by baseline (TRIG BL) adjustment R26. This trim pot sets the current through Q7, and therefore Q6, such that the gate-source voltage of Q6 plus the drop across CR9 is equal and opposite to the base-emitter drop of Q9, causing the two voltages to cancel each other.

4.6.5 Comparator

The comparator (ref: schematic 0103-00-1116 sheet 2) which is made up of current source Q8 and differential pairs Q12/Q13 and Q14/Q15, detects the peak of the triangle and produces two square wave outputs. One square wave output from the comparator (Q15 collector) drives the switch buffer, while a second square wave of opposite phase (Q14 collector) drives the square buffer. Output transistors Q14 and Q15 have different values of collector and emitter resistors to match the input requirements of the buffer that each drives. The comparator's threshold voltage is developed by the positive (+ COMP) or negative (− COMP) current from the high frequency compensation circuit. The appropriate current is selected by switch U22, and the

voltage drop across R48 created by this current becomes the comparator threshold voltage.

As the triangle voltage at the base of Q13 reaches the positive threshold voltage (+1V) set by U22 pin 2, Q13 turns on as Q12 turns off. When Q12 and Q13 switch, they also cause the second differential pair, Q14 and Q15, to switch. As Q15 switches "off", current through R38 decreases and the collector of Q15 goes low (about −1.6V as determined by R35). The switch buffer, driven by this negative voltage, switches the threshold voltage at the base of Q12 from +1V to −1V and causes the triangle to switch from a rising to a falling slope. As the triangle voltage at the base of Q13 reaches the negative threshold, both differential pairs switch states, turning on Q12 and forcing the collector of Q15 high as it also turns on. Thus the triangle is switched to its rising slope and the threshold voltage is reset to +1V. In this manner, triangle and square waveforms are continuously generated in a loop.

CR57 and CR58 increase the transistor switching speed of Q14 and Q15 by limiting the signal swing at their bases to about 0.7V. Resistors R39 and R41 increase the switching speed of Q14 and Q15 by providing a small current which keeps them from turning entirely off, and diodes CR18 and CR19 are switched on and off to further guarantee that Q14 and Q15 do not switch off.

Diode array (U22 at pins 5, 6, 8), operates in a similar manner to the current switch. The switch buffer output (U22 pin 6) state determines the polarity of the comparator threshold at pin 2. The comparator threshold voltage at pin 2 is limited to ±1V by the voltage drop across the 332Ω resistor (R48) since the +COMP and −COMP currents supply no more than 3 mA. The high frequency compensation circuit reduces the +COMP and −COMP currents on the highest frequency range which lowers the comparator threshold voltage at the base of Q12 to compensate for switching delays (see High Frequency Compensation).

4.6.6 Switch Buffer

The switch buffer (ref: schematic 0103-00-1455 sheet 2) shifts the level of the comparator's square wave to provide a voltage excursion (±2.2V) capable of driving the two current switches in the generator loop. The circuit consists of a push-pull emitter follower (Q10, Q11) biased on by the voltage drops across CR16 and CR17 and controlled by the comparator output at the collector of Q15. The ±2.2V square wave output simultaneously controls the current switch in the generator loop and the polarity of the comparator threshold voltage.

4.6.7 High Frequency Compensation

The High Frequency Compensation (ref: schematic 0103-00-1455 sheet 1) circuit decreases both triangle peak levels on the highest frequency range to compensate for comparator switching delays. This is accomplished by adjusting two constant currents (+COMP and −COMP) in proportion to the programmed frequency. These currents develop the generator loop comparator threshold voltage by alternately flowing through R48 in the comparator circuit.

From the lowest frequency through 999kHz, U26 pin 10 is open, leaving R66 disconnected. R67 holds U23 pins 12 and 13 and the emitter of Q20 at 0.0V. This puts 15V across series resistors R62 and R65 and −6.8V at the base of Q18. 7.5V is now across R63 and Q18 has a collector current of 3mA. The same current that flows through R65 also flows through R60. Since about 1.4V is dropped across CR72 and CR73, there will be about +6.8V at the base of Q19. The emitter of Q19 is +7.5V which causes about 3.0mA to flow from the collector of Q19 through U22 and R48 to ground during half of the cycle setting up a +1V threshold voltage at the base of Q12. On the opposite half of the cycle, the base of Q12 switches to −1V because the same amount of current (3.0mA) flows from ground through R48 and U22 to the collector of Q18.

In the 1MHz to 12MHz frequency range, U26 pin 10 is connected to R66. At top of the range, 0.2mA is sourced from ground through R67 to pin 7 of U23 (in the VCG), lowering the voltage at U23 pin 12 to about −8.8V. This decreases the voltage at the emitter of Q20, as well as the current through R62, R65, and R60 which forces the bases of Q19 and Q18 closer to their respective power supply voltages. The current through R48, the collectors of Q19 and Q18, and the threshold voltage at the base of Q12 are all decreased. This new lower threshold voltage causes the square wave to switch earlier than normal, maintaining the triangle peaks at the same levels as on lower ranges. If the generator is not at full scale, a voltage inversely proportional to the frequency is set at the base of Q12.

4.6.8 Square Buffer

The square buffer consisting of Q16 and Q17, and associated circuits (ref: schematic 0103-00-1455 sheet 2) buffers the square wave from the function generator loop (Q14 collector). The output ($\overline{\text{SWSQR}}$) drives the trigger logic, low frequency waveform synthesizer, and square selector. The square buffer is similar to the switch buffer (ref: paragraph 4.6.6) except for output phasing and output level. Square buffer output is TTL compatible. A highly differentiated portion of HFSQ is coupled

through C49 to the triangle node. This signal counteracts switching transients which are coupled through the current switch diode bridge.

4.6.9 Trigger Logic

The trigger logic circuit (ref: schematic 0103-00-1455 sheet 3) allows the function generator loop to be triggered or gated from an external TTL signal. When the trigger circuit is enabled by a logic high on the MC0 line and no trigger input has occurred, the generator is prevented from running by sinking away current (Ref. paragraph 4.6.1) from the triangle node (TRN) that would normally charge the timing capacitor. Selection of triggered or gated mode is determined by logic line MC1, which is low for triggered mode, high for gated mode. Triggering the generator releases TRN which allows the loop to run until $\overline{\text{SWSQR}}$ completes one complete cycle (triggered mode) or until the trigger signal is released and the last cycle begun is completed (gated mode). In addition, the waveform synthesizer output at U2 pin 11 must also be high to stop the generator when the Frequency is 1.1 kHz or lower. $\overline{\text{KILL}}$ inhibits the generator when in DC function.

The following paragraphs describe the relationship in various conditions relative to the trigger logic.

Continuous Mode: In Continuous Mode, U18 pin 1 (MC0) is low which holds U18 pin 3 low and sets U10 pin 5 high. If DC function is not selected, $\overline{\text{KILL}}$ (U2 pin 9 and U3 pin 4) will be high and U2 pin 8 (U3 pin 1) will be low. With U3 pin 1 low and pin 4 high, U3 pin 6 (RUN) is cleared high allowing the generator to free-run.

Trig Mode: In trigger mode, U9 pin 4 (MC1) is held low, forcing U9 pin 6 high and U18 pin 1 (MC0) is held high, making U10 pin 4 high. The square wave output, $\overline{\text{SWSQR}}$ toggles high or low with each half cycle. For this portion of the discussion, $\overline{\text{SWSQR}}$ (U2 pin 5) is low, making U2 pin 6 high. TRIG EN (U9 pin 10) from the microprocessor remains high except during a TRIG SLOPE change. With U9 pin 10 high, U9 pin 8 is low and U10 pin 1 goes high. Thus, U10 pins 1 and 4 are neither set nor cleared.

There are 4 possible combinations of the TRIG SLOPE control line (U11 pin 1) and Trig In connector (U11 pin 2) which control U11 pin 3. These will be explained later, but for this discussion U11 pin 3 is high. Since U11 pin 3, and U10 pins 1 and 4 are all high, pin 5 (Q) remains high. With the generator in a function other than DC, U2 pin 9 ($\overline{\text{KILL}}$) is high and U3 pin 1 is low. For frequencies greater than 1kHz, LF (U2 pin 1) is low and U2 pin 3 high. With U3 pin 1 low and pin 4 high, U3 pin 6 (RUN) remains high and the generator loop continues to run.

When $\overline{\text{SWSQR}}$ toggles high, U2 pin 6 goes low, U9 pin 8 switches high and U10 pin 1 is driven low. This forces U10 pin 5 low and U2 pin 8 high. As before, U3 pin 6 does not change, and the generator loop continues to run. However, U3 pins 1 and 4 are now neither set nor cleared. This arms the clock input for a rising edge, making the $\overline{\text{Q}}$ output opposite of the D input, which is held high by the low on U2 pin 1.

On the next transition of $\overline{\text{SWSQR}}$, U2 pin 5 goes from high to low and U2 pin 6 goes low to high, clocking U3 pin 3 and making U3 pin 6 (RUN) go low. This disables the generator loop as the positive slope of the triangle reaches 0 volts. On this phase of $\overline{\text{SWSQR}}$, U9 pin 8 goes low and U10 pin 1 goes high, arming U10 pin 3 for a rising edge clock.

Generator Triggering: The triggering path is from U11 pin 3 (U10 pin 3) through U10 pin 5, U2 pin 8 and U3 pin 6. The generator is triggered with a pulse at either of the two trigger sources. These are the Trig In connector (U11 pin 2) from the front panel and the TRIG SLOPE control line (U11 pin 1) from the microprocessor. The four possible combinations of U11 pins 1 and 2 are shown below, along with the result at pin 3. U11 pin 1 is low for Positive Trigger Slope and high for Negative Trigger Slope.

U11-1	U11-2	U11-3
L	L	L
L	H	H
H	L	H
H	H	L

The trigger source pulse must produce a positive going transition at U11 pin 3 (and therefore U10 pin 3). To insure that U10 pin 5 toggles high, a complete cycle of the trigger source is desired. When U11 pin 3 makes a positive transition, U10 pin 5 goes high and U2 pin 8 toggles low, switching RUN high and allowing the generator to cycle. When the triangle reaches its positive peak, $\overline{\text{SWSQR}}$ toggles high, making U9 pin 9 low, pin 8 high and U10 pin 1 low. This forces U10 pin 5 low and U3 pin 1 high. On the next transition of $\overline{\text{SWSQR}}$, U2 pin 6 goes high, causing U3 pin 6 to return low, disabling the generator as the positive slope of triangle reaches 0 volts. Only one cycle of generator output is enabled for each trigger pulse applied.

Gated Mode: The trigger mode description should be read and understood prior to reading this paragraph because all logic levels previously discussed apply here except for U9 pin 4 (MC1). In gate mode, the generator output is continuously enabled for the entire duration of the applied trigger signal. MC1 is high and the levels at U9 pin 6 and U18 pin 3 are inverted with respect to U11 pin 3. This becomes the alternate triggering path between U11 pin 3 and U10 pin 5. When U11 pin 3 goes high, U10 pin 4 switches low which forces pin 5 high. U2

pin 8 goes low and U3 pin 6 (RUN) toggles high, allowing the generator to oscillate. U10 pin 5 and U3 pin 6 (RUN) will remain high as long as U11 pin 3 is high.

Manual Trigger: Bus or front panel manual triggering is accomplished by maintaining TRIG EN high while toggling the TRIG SLOPE line to the opposite state, then back to the original state. This will always produce a clock transition at U10 pin 3.

Slope Change: When a slope change is to be made, the TRIG EN line from the microprocessor goes low to prevent the slope change from spuriously triggering the generator in trigger mode. If the change is made with the generator quiescent, U9 pin 9 is high, making U9 pin 8 high and U10 pin 1 low. Because U10 pin 4 is always high, a low at pin 1 maintains U10 pin 5 low, regardless of what occurs at pin 3 due to a change at U11 pins 1 and 2. When the slope change has been completed, TRIG EN (U9 pin 10) returns high, allowing a trigger from U11 pin 3 to pull U10 pin 5 high.

Low Frequency: When the Frequency range is 1.1 kHz or lower, the trigger logic works much the same as previously described, except that U3 pin 2 must be brought high to stop the generator. This occurs at either the zero crossing of the rising edge of the triangle (Haver Off), or at the negative peak of the triangle (Haver On). If Haver is Off, U20 pin 9 (Waveform Synthesizer) functions as a zero crossing detector that controls the trigger logic. If Haver is on, U5 (Waveform Synthesizer) acts as a negative peak detector. U2 pin 11 goes low in either condition until a detector is satisfied. With U2 pin 11 high, the next positive transition at U10 pin 11 forces $\overline{Q}$ (U10 pin 8) low. For the 5 lowest frequency ranges, LF (U2 pin 1) is high, making pin 3 high and causing U2 pin 3 to go low. As long as U2 pin 3 is low, the generator will run continuously once triggered on. The generator can therefore be stopped at the end of a 1000 point synthesized waveform by controlling this line.

Haver Off: When Haver is Off, HAV (U19 pin 13) is low, which disables U5 and maintains U2 pin 13 high. The zero crossing detector (U20 pin 9) controls the trigger logic; see Low Frequency above.

Haver On: When Haver is on, U19 pin 13 (HAV) is high which disables the zero crossing detector (U20 pin 9). Thus, with HAV high, U5 pin 6 detects the negative peak and controls the trigger logic.

DC Function: DC function overrides any other signal used to control the trigger logic circuit. When DC is selected, the microprocessor forces U2 pin 9 ($\overline{KILL}$) low. This causes U3 pin 6 (RUN) to also go low, disabling the generator loop as the positive slope of the triangle reaches 0 volts.

4.7 FREQUENCY SYNTHESIZER

The frequency synthesizer (ref: schematic 0103-00-1454 sheet 2) is shown in figure 4-7 and includes the internal functions of the PLL IC, U22. These functions include the reference oscillator, reference divider (– 6144), variable divider (– N), phase detector and internal registers and latches. When in synthesizer mode, the frequency synthesizer generates the signal used to internally clock the function generator loop. The Phased Locked Loop (PLL) within the frequency synthesizer (bold arrows) consists of the PLL IC U22, Low Pass Filter (LPF) U23A, 2 pole filter U23B, 32-64 MHz VCO (Q5 through Q10), divider U25 and U26, and selector U24. The PLL circuit operates over the frequency range of 1MHz to 16MHz in 1kHz steps and 16MHz to 32MHz in 2kHz steps

The PLL circuit as a whole operates in the following manner.

1. The phase detector compares the frequency and phase of the variable (– N) divider output to a fixed 1 kHz reference frequency from the reference (– 6144) divider
2. The phase detector, loop filter and 2 pole filter generate a dc VCO control voltage that changes as required to drive the VCO frequency to exactly N times the 1 kHz reference. When this occurs, the outputs of the reference (– 6144) and variable (– N) dividers are at the same frequency and phase, locking the loop
3. The VCO output frequency at the emitter of Q10 is prescaled by five – 2 series flip-flops, U25 and U26. The programmable selector (U24) selects the appropriate signal to be input to the variable (– N) divider (U22 pin 9). The divider output is applied to one input of the phase detector.
4. The loop will remain locked with the VCO at a given frequency until the variable division ratio N is changed.

The reference oscillator uses an external crystal (Y1) to generate a 6.144 MHz reference frequency. The reference divider is hard-wired (at pins 1, 2 and 18) for a division ratio of 6144. The 6.144 MHz reference frequency is divided by 6144, and the resulting 1 kHz reference is applied to one input of the internal phase detector. The variable divider (– N) is programmed by serial data at the pin 11 DATA input. This data is clocked into a 16-bit internal shift register by low-to-high transitions on the pin 10 CLK line. The first two bits control internal switches which are used to control the prescaler selector U24. The remaining 14 bits are a binary representation of the – N division ratio, and are loaded most significant bit first. When the serial load is com-

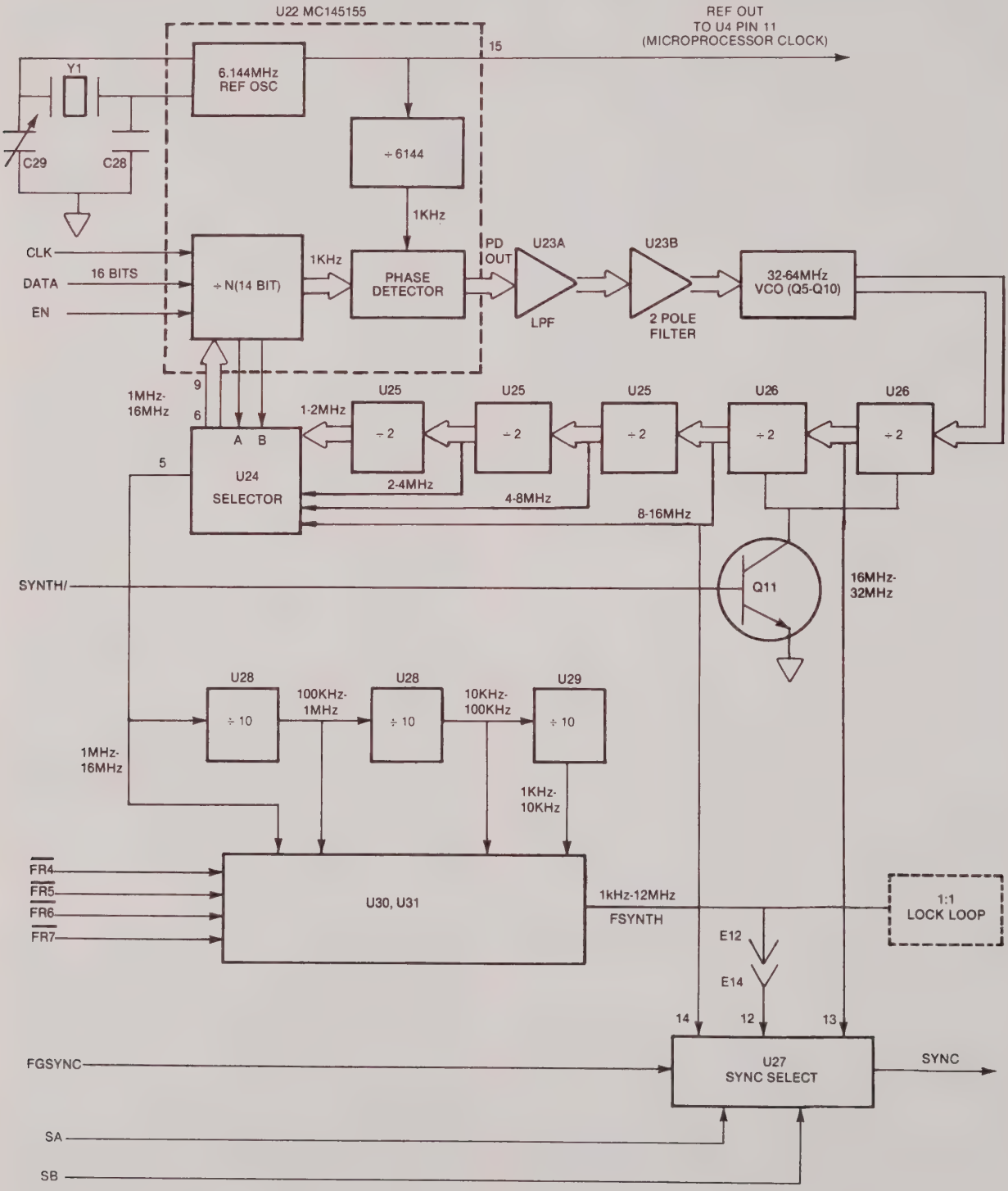


Figure 4-7. Frequency Synthesizer Circuit

plete, a logic high on the pin 12 EN line latches the data in the shift register into the programmable ÷ N counter. The output of the ÷ N counter is applied to the second input of the internal phase detector, and is also at 1 kHz when the loop is locked.

A high on the $\overline{\text{SYNTH}}$ line (originated by the microprocessor and latched by data latch U14) brings the collector of Q11 low, disabling the synthesizer and initializing the ÷ 2 dividers by clearing all of the internal flip-flops. When frequency synthesizer mode is selected, this line goes low and the flip-flops are enabled.

The internal phase detector is a digital tri-state device. It produces negative-going pulses when the variable frequency is greater than the reference frequency or is leading it in phase, and positive-going pulses when the variable frequency is less than the reference frequency or is lagging in phase. The output is in a high-impedance state when the two signals are of equal frequency and phase.

Loop filter U23A converts the positive-going and negative-going pulses from the U22 phase detector to a steady dc frequency control voltage. The filter time constant is determined by C32 and R30, and damping by R33. A high frequency bypass capacitor (C33) is used to reduce noise in the filter. The voltage divider consisting of R31 and R32 sets the voltage at U23A input pins 2 and 3 to 1.25 Vdc.

Two pole filter U23B further reduces the noise on the dc voltage before applying it to the VCO.

At the input of the VCO are 5 voltage controlled varactor diodes which determine the instantaneous frequency of the tuned circuit (Q5/Q6, L1/L2). The output of this oscillator, through R42, drives the buffer amplifier consisting of Q7 through Q10.

The output frequency is established by the value of the inductors and the capacitance of the varactor diodes which vary with the voltage applied at R38. Output frequency increases with an increase in the frequency control voltage.

The VCO signal is divided by the selected prescalar ratio (between 2^2 and 2^5) in U25 and U26 to yield the desired output frequency. This allows a one octave of change of 32 to 64 MHz to produce a 1MHz to 16MHz frequency range.

The same signal which provides the loop input to the ÷ N divider at U22 pin 9 is sent from U24 pin 5 to the divider/selector circuits U28 through U31. This signal is divided by three ÷ 10 series counters, U28 and U29. The programmable selector (U30/U31) selects the appropriate signal to be input to the 1:1 lock loop (ref: paragraph 4.8) as FSYNTH.

The sync select, U27 selects one of four signals to drive both the TTL and ECL sync outputs. The output is determined by the logic levels of SA and SB from U14 of the analog interface. For frequencies less than 1kHz, the square selector on the waveform generator board chooses the square wave from the waveform synthesizer, which enters the microprocessor/synthesizer board as FGSYNC. Between 1kHz and 12MHz, the coax cable FSYNTH provides the sync drive signal. From 12MHz to 16MHz, U27 selects pin 14, and from 16MHz to 32MHz pin 13 is selected. The output, SYNC, goes directly to the sync out drivers on the waveform generator board.

4.8 1:1 LOCK LOOP

When the synthesized mode is selected, the 1:1 lock loop provides a correction voltage (VLOOP) to the VCG which maintains the function generator loop frequency within the synthesized frequency specification. This is done by monitoring the frequency stable input from the frequency synthesizer (FSYNTH) and the function generator loop frequency (HFSQ), then providing an instantaneous dc voltage at VLOOP to increase or decrease the HFSQ frequency until it matches the FSYNTH frequency.

As shown in figure 4-8, the 1:1 lock loop consists of a phase detector (U29), charge pump (U28) and switchable low pass filter (U32). The phase detector monitors the

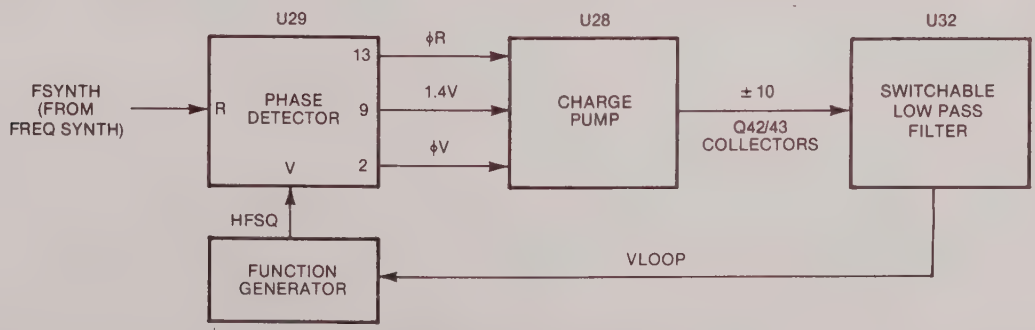


Figure 4-8. 1:1 Lock Loop

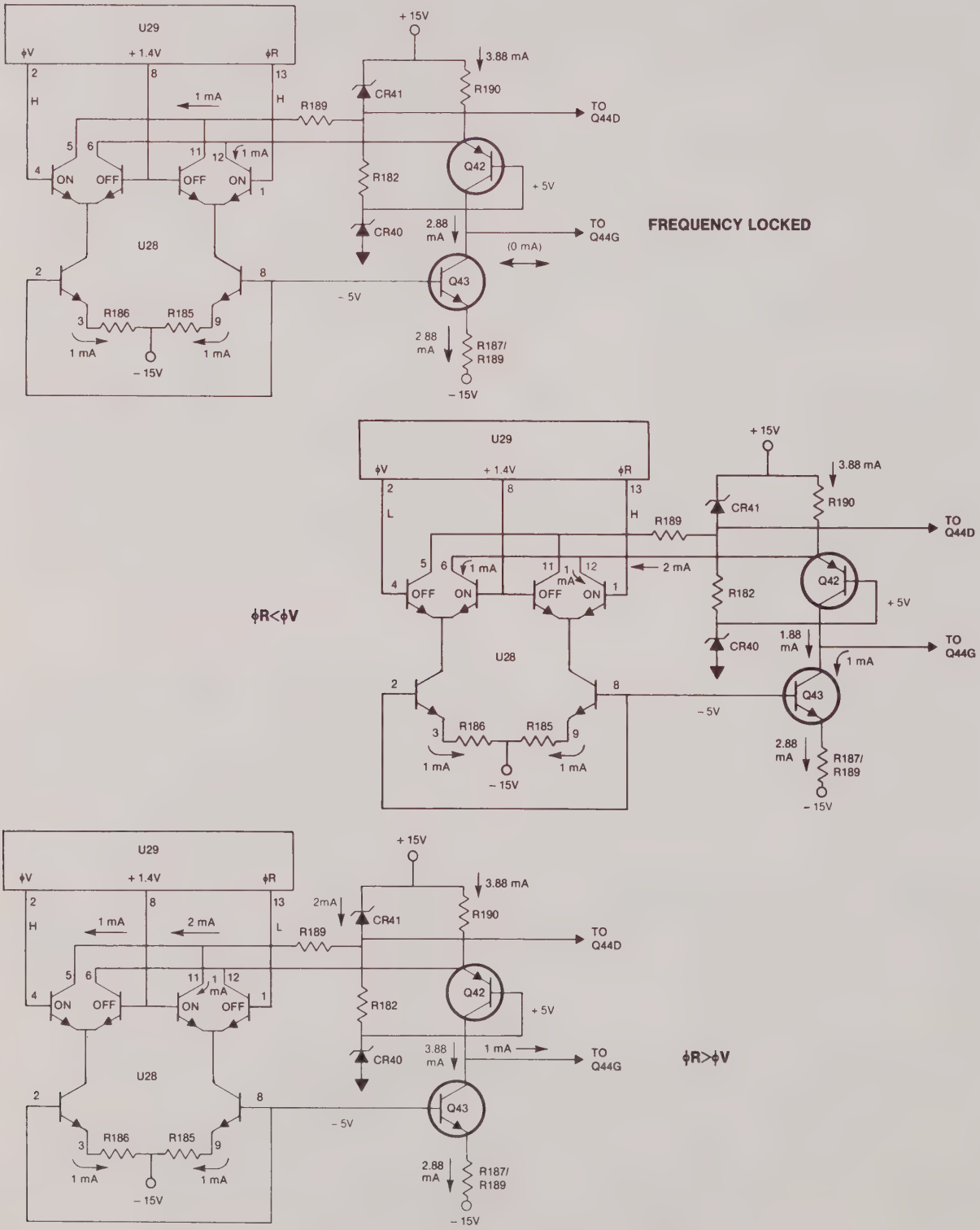


Figure 4-9. Charge Pump Current Flow

FSYNTH (R) and HFSQ (V) inputs, then provides one of three possible output combinations of ϕR and ϕV. These outputs are either more positive (H) or more negative (L) than the reference voltage of +1.4V at the phase detector output (U29 pins 8 and 9). The conditions for each possible combination of ϕR and ϕV are as follows:

CONDITION	ϕR	ϕV
Frequency Equal:		
In phase	1 (H)	1 (H)
ϕ_R leads ϕV	Neg. Pulse (L)	1 (H)
ϕ_R lags ϕ_V	1 (H)	Neg. Pulse (L)
Frequency Unequal:		
$\phi_R > \phi_V$	0 (L)	1 (H)
$\phi_R < \phi_V$	1 (H)	0 (L)

For the remainder of this discussion, refer to figure 4-9 and schematic 0103-00-1455 sheet 6. The bases of Q42 and Q43 are set at +5V and −5V respectively, and constant currents flow through the following points in the charge pump circuit:

Point	Current (mA)
R190	3.88
Q43 collector	2.88
U28 pin 3	1.0
U28 pin 9	1.0

Depending on the combination of ϕR and ϕV, the total amount of current flowing through U28 pins 6 and 12 can be 0mA, 1mA or 2mA. This current is tapped from the 3.88mA that originates from the +15V supply through R190. When frequency lock is established, ϕR and ϕV are both high. U28 pin 5 sinks 1mA from the +15V supply through CR41 and R189, which satisfies the 1mA requirement of U28 pin 3. U28 pin 12 sinks an additional 1mA from R190 to satisfy the 1mA requirement of U28 pin 9. A total of 2.88mA from R190 remains to flow through Q42, with Q43 taking it all and leaving no current to be supplied to or drawn from the selected low pass filter components at the gate of Q44. Thus, the voltage at the gate of Q44 is not charged up or down.

When ϕR is low and ϕV is high, U28 pins 5 and 11 each sink 1mA from CR41 and R189, satisfying the 1mA requirements of U28 pins 3 and 9. No current flows through U28 pins 6 and 12 because these transistors are now off. This means that all the current supplied by R190 (3.88mA) flows through Q42. Because Q43 can only accept 2.88mA, the excess (1mA) flows into the selected flow pass filter components at the gate of Q44, charging this point positive.

When ϕR is high and ϕV is low, no current flows through U28 pins 5 and 11 because these transistors are now off. U28 pins 6 and 12 each sink 1mA through R190, satisfying the 1mA requirements of U28 pins 3 and 9. Because U28 draws a total of 2mA from R190, only 1.88mA is left to flow through Q42. The additional 1mA needed to satisfy the 2.88mA requirement of Q43 is drawn from the selected low pass filter components at the gate of Q44, charging this point negative.

The low pass filter section contains three switchable filters and one fixed filter to dampen the charge pump output signal and provide a dc voltage at VLOOP. In each of the three switchable ranges (4, 5 and 6), the respective digital control line ($\overline{FR4}$, $\overline{FR5}$ and $\overline{FR6}$) goes low, connecting an R/C filter. In the highest range (7), only the fixed filter consisting of R194, C108 and C109 (and any stray capacitance in the circuit) is connected. This filter has negligible effect on the other three ranges. FET Q44 provides a high input impedance to the filter and charge pump circuits, while Q45 in an emitter follower configuration, provides a low impedance to the VCG at VLOOP.

4.9 WAVEFORM SYNTHESIZER

The waveform synthesizer produces the digitally synthesized waveforms for the Func Out at frequencies 1 kHz and below. It consists of seven circuits: ÷1/÷100 counter, ÷1000 up/down counter, data selector, waveform EPROM, latch, and DAC, as shown in figure 4-10 and schematic 0103-00-1455 sheet 3.

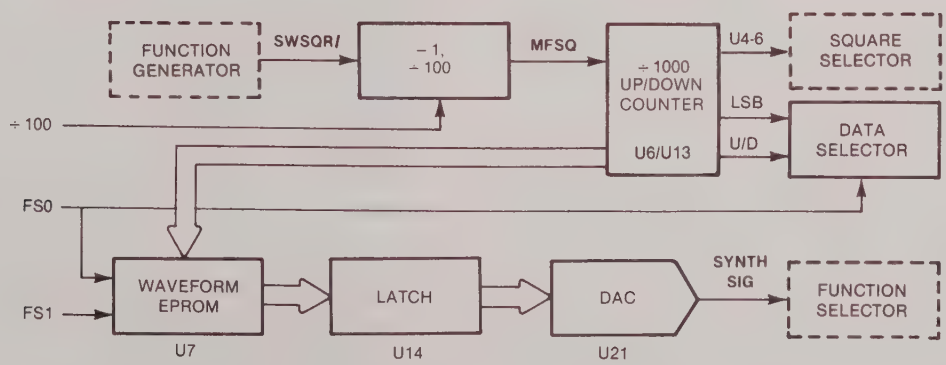


Figure 4-10. Waveform Synthesizer Block Diagram

Table 4-3. Internal Reference Selection

Frequency Range	Generator Loop Frequency (HFSQ)	÷1/÷100	Medium Frequency Square Wave (MFSQ)
.100 to 1.000 kHz	.100 to 1.000 MHz	÷1	.100 to 1.000 MHz
10.0 to 99.9 Hz	10.0 to 99.9 kHz	÷1	10.0 to 99.9 kHz
1.00 to 9.99 Hz	1.00 to 9.99 kHz	÷1	1.00 to 9.99 kHz
.100 to .999 Hz	10.0 to .999 kHz	÷100	.100 to .999 kHz
10.0 to 99.9 mHz	1.00 to 9.99 kHz	÷100	10.0 to 99.9 Hz

The output frequency of the synthesizer is 1/1000 of the range selected. In addition, in the 2 lowest ranges, $\overline{\div 100}$ is low, further dividing this signal by 100.

The internal reference originates from the function generator loop at $\overline{\text{SWSQR}}$ and clocks the 9-bit up/down counter. This signal must pass through the ÷1/÷100 divider (U16; ref: schematic 0103-00-1455 sheet 3) where the frequency is either divided by 1 or 100, depending upon the selected frequency range, see table 4-3.

The 9-bit up/down counter (U4, U6, and U13) counts from 0 to 499, then reverses and counts from 499 to 0. The counter steering circuit (U5, U11, and U12) watches for the top and bottom counts, then reverses the direction of the counter. When the counter increments, U3 pin 12 is low and pin 8 is high. At the top count, U19 pin 10 toggles high, disabling the counter for one cycle. Also at the top count, U3 pin 12 goes high and on the next clock pulse from MFSQ, U3 pin 8 (the counter up/down control line) goes low, causing the counter to begin to decrement, returning U19 pin 10 to its original low state. At the bottom count, U19 pin 10 again goes high, disabling the counter for one cycle. U3 pin 12 goes low, and on the next clock pulse from MFSQ, U3 pin 8 goes high, causing the counter to begin to increment. U19 pin 10 again returns low.

The counter output drives the inputs of EPROM (U7) which contains the data needed to produce the sine, triangle, ramp up, and ramp down waveforms. The status of lines FS0 and FS1 determine the waveform by selecting which block of data as accessed; see table 4-4. For sine and triangle waves, the EPROM produces one half cycle, negative to positive peak, on the up count (0 to 499), then uses the same data in reverse, positive to negative peak, on the down count (499 to 0). The data from the EPROM (U7), is latched through U14 to DAC U21.

Table 4-4. EPROM Control Lines

FS0	FS1	Function
0	0	DC
0	0	Sine wave
0	1	Triangle
1	0	Ramp up
1	1	Ramp down

The DAC converts the data from the EPROM into a current, SYNTH SIG, for the function selector.

The synthesizer can also produce ramp up and ramp down waveforms. These ramps are stored in the EPROM (U7), as are the sine and triangle waveforms. To produce the ramps, the line FS0 goes high. The line FS1 selects either the ramp up (FS1 low) or ramp down (FS1 high). In generating the ramps, the up/down counter functions the same as it does for triangles and sine waves; counting 0 to 499 and 499 to 0, except that the least significant bit to the EPROM is controlled by the data selector (U11, U18). The U/D line (U3 pin 9) is the complement of the line that causes the counter to count up or down. When counting up, U/D is low, which holds the least significant bit low. This allows only even addresses to be accessed. When counting down, U/D is high, the least significant bit is held high, and only odd addresses are accessed.

Divider (U17) is the ÷100 counter and U16 selects either ÷1 or ÷100 for the waveform synthesizer block.

4.10 OUTPUT BLOCK GENERAL DESCRIPTION

The output block, shown in figure 4-11, consists of the square selector, square shaper, sine converter, function selector, preamplifier, XY multiplier, output amplifier, and attenuator. It selects, amplifies and provides offset

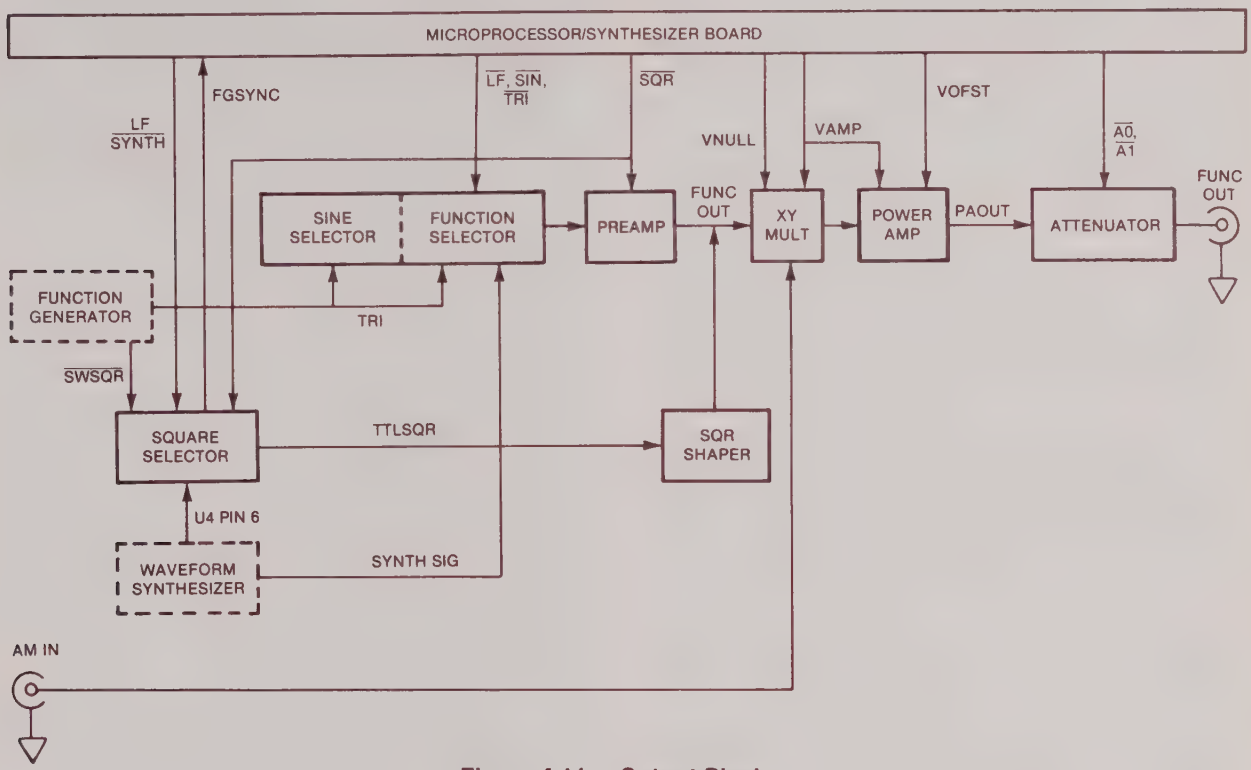


Figure 4-11. Output Block

for the appropriate waveform before reaching the Func Out connector.

The function selector circuit chooses the triangle wave (TRI) from the function generator, the waveform synthesizer output (SYNTH SIG, for frequencies of 1 kHz and below, not square function), or sine wave derived from the triangle wave by a sine converter in the function selector circuit. The output of the function selector is buffered by the preamplifier before entering the XY multiplier. If square function is selected, the square signal from the square selector is modified by the square shaper which drives the XY multiplier. For frequencies of 1 kHz and below, the waveform synthesizer square wave output at U4 pin 6 is selected by the square selector. The X-Y multiplier circuit takes the output from the preamplifier or square shaper, then varies the waveform amplitude in proportion to amplitude control voltages VAMP and VNULL from the sample and hold section of the microprocessor board.

The output amplifier provides the final gain and output drive capabilities for the waveform, and sums offset signal (VOFST) into the waveform as required. The attenuator provides 20 dB and 40 dB of attenuation for the output waveform before reaching the Func Out connector.

4.11 OUTPUT BLOCK DETAILED DESCRIPTION

4.11.1 Sine Converter

The sine converter, which is part of the function selector (ref: schematic 0103-00-1455, sheet 4), transforms the triangle waveform into a sine wave by using the logarithmic response characteristics of the six matched diodes (CR66, CR67, CR68, CR69, CR70, CR71) to approximate a sine wave current output. The triangle output (TRI) enters the converter at R116. SIN DIST A trim pot (R113) adjusts the converter input for triangle amplitude variation. Two other adjustments, SIN DIST B and SIN DIST C (R100 and R105), balance the positive and negative peaks respectively. The SIN OFST trim pot dc balances the sine output waveform. Current output is switched through U30 when $\overline{\text{SIN}}$ is low.

4.11.2 Function Selector

The control lines $\overline{LF}$, $\overline{SIN}$ and $\overline{TRI}$ at the function selector circuit (ref: schematic 0103-00-1455, sheet 4) determine which waveform is connected to the preamplifier input by the 4 section CMOS analog switch U30. Respectively, these are the waveform synthesizer output signal (SYNTH SIG), sine convertor output and triangle (TRI). For square selection, refer to Square Shaper paragraph 4.11.6.

In this description of the analog switch, component designations refer to the section that controls the triangle signal. Except for signal names and component numbers, the 2 remaining sections are identical and need no further discussion. When the triangle signal (TRI) is selected, $\overline{TRI}$ goes low, which connects pins 10 and 11 together by turning on a mosfet. Digital noise on the control line (which could be coupled to the output through the mosfet gate capacitance when the analog switch is open) is reduced by C84 and C88. Tri Level trim pot (R161) adjusts the triangle waveform current that enters the analog switch.

When either the triangle or sine waveforms are not selected, the FET switches (U30) are provided with increased isolation by shorting the inputs to ground through Q25 and Q27 respectively. For example, when $\overline{TRI}$ is high (not selected), Q26 is turned off and the collector of Q26 goes low, forward biasing Q25. This effectively shorts the emitter and collector of Q25 together, sending the triangle signal at this point to ground.

4.11.3 Preamplifier

The preamplifier (ref: schematic 0103-00-1116 sheet 4) consists of separate low frequency and high frequency amplifiers. The low frequency path, which also establishes dc stability, is provided by Q36, Q29 and Q30. R150 sinks a total of 4mA through the emitters of differential amplifier Q36. The collector current in the left hand transistor in Q36 is mirrored by the collector current of transistor Q29, which added to the small base current of Q30 provides collector current for the right hand transistor. The bases of Q31 and Q32 are held at plus and minus 6V, which results in Q31 being a current source and Q32 a current sink. R131 sources a constant current of 5.5mA and R151 sinks a constant current of 3.3mA.

If the input current from the function selector at the junction of R134 and R136 is zero, the current through the differential amplifier (Q36) will be balanced with 2mA in each side. The base of Q30 is at approximately + 5.5V with 2.2mA sunk through R137. In this condition, the total amount of current sourced by R131 (5.5mA) is split between R137 (2.2mA) and R151 (3.3mA). The amount of emitter current available for Q31 is determined by the current through R131 minus the current through R137. Equilibrium is reached when the collector current of Q31 plus the base current of Q33 equals the Q32 collector current. At this time the output voltage at the junction of R140 and R134 can be set to exactly zero with R147.

When the function selector output goes positive, current is sourced into the preamplifier at the junction of R134 and R136 (the current summing node), increasing the right hand side Q36 base voltage. This voltage increase causes an imbalance in Q36, with the right hand side emitter sinking more than 2mA, and the left hand side emitter current sinking an equal amount less than 2mA to maintain the current through R150 at 4mA. Reducing current in the left hand side of Q36 lowers the voltage drop across R128, increasing the voltage at the base of Q29 and decreasing the current through its collector. With an increased need for collector current in the right hand transistor of Q36 and, at the same time, a decrease in Q29 collector current, the difference is supplied by the base of Q30. The small change in Q30 base current translates to a larger emitter current change which increases the voltage drop across R137 and lowers the Q30 base voltage below + 5.5V. The current through R137 is now greater than 2.2mA which limits the current to Q31. R151, which is still sinking 3.3mA, now sinks more than Q31 is sourcing. The difference in current is taken up by current through the emitter and base of Q33. This current originates from R134 and lowers the voltage at the junction of R134 and R140, forcing the output voltage negative. Equilibrium is reached when R134 sinks the same current sourced by the function selector at the summing node.

When current is sunk by the function selector at the junction of R134 and R136, this whole process is reversed producing a positive output voltage. Thus it can be seen that the junction of R136/R134 is a current summing junction and the preamplifier is an inverting amplifier acting as a current to voltage converter.

The high frequency amplifier input signal is fed forward by C69 and C70 to Q31 and Q32. Emitter follower Q33 provides a low impedance output for the amplifier before entering the XY Multiplier input.

4.11.4 Square Selector

The square selector (ref: schematic 0103-00-1455 sheet 3) determines which of two square wave sources (low frequency square wave from the synthesizer U4 pin 6 and $\overline{SWSQR}$ from the square buffer), will feed the three square selector outputs. The outputs are HFSQ which drives the 1:1 lock loop, FGSYNC which can be used by the frequency synthesizer for possible selection to drive

the TTL Out and ECL Out connectors, and TTLSQR which drives the square shaper.

For frequencies at or below 1kHz, control line LF is TTL logic high which makes U8 pin 10 low and U8 pin 5 high. This causes the low frequency square wave from the synthesizer (U4 pin 6) to be inverted at U8 pin 11, pin 6 and again at U15 pin 8 before going to the frequency synthesizer as FGSYNC. A logic low at the LF control line blocks the low frequency square wave from the synthesizer (U4 pin 6) by making U8 pin 11 high. It also causes the square wave from $\overline{\text{SWSQR}}$ to be inverted at U8 pin 8, pin 6 and again at U15 pin 8 before going to the frequency synthesizer as FGSYNC.

If the square wave function has been selected, $\overline{\text{SQR}}$ is low, making U5 pin 2 high and inverting the signal from FGSYNC before being sent to the Square Shaper as TTLSQR. For all functions other than square wave, $\overline{\text{SQR}}$ is high, disabling TTLSQR (U5 pin 12).

If frequency synthesizer Mode has been selected, $\overline{\text{SYNTH}}$ goes low, making U8 pin 1 high and inverting the $\overline{\text{SWSQR}}$ signal at pin 3 before entering the 1:1 Lock Loop circuit as HFSQ.

4.11.5 Square Shaper

The square shaper (ref: schematic 0103-00-1455 sheet 4) accepts a TTL square signal (TTLSQR) from the Square Selector when square wave has been selected. The TTLSQR signal is converted to a clean, fast square wave by alternately sourcing and sinking current through R154. The Square Shaper output signal drives the XY multiplier.

TTLSQR is shifted to a bipolar square signal by R119, R120, R121 and R124, then applied to the bridge circuit formed by Q23, Q24, CR31 and CR32. When TTLSQR is high, Q24 is turned off, forward biasing CR31 and allowing current from the + 15V supply to flow through R117, R122 and CR31. This develops the upper level square across R154. At the same time, Q23 is sourcing current through R123 and R118 to − 15V, reverse biasing CR32. A low TTLSQR turns Q23 on and Q24 off, reversing the situation and developing the lower level square across R154.

When a function other than square is selected, $\overline{\text{SQR}}$ is high. This allows the gate of Q37 to be pulled high by R155, turning "on" Q37 and connecting the output of the preamp to FUNC OUT. At the same time, the gate of Q48 is pulled low by R153, turning "off" Q48 and preventing the square shaper output from reaching FUNC OUT. When square function is selected, $\overline{\text{SQR}}$ goes low, shorting analog switch U30 pins 2 and 3. This turns Q37 "off", disconnecting the preamp output from FUNC OUT. In addition, Q34, Q35 and Q48 are turned "on", connecting the square shaper output to FUNC OUT.

4.11.6 X-Y Multiplier

The X-Y multiplier (ref: schematic 0103-00-1455 sheet 3) is a transconductance multiplier that drives the output amplifier with differential currents at U31 pins 2 and 14. These currents are derived from the function signal at FUNC OUT, which enters U31 as the X input. The magnitude of the current difference at the output is directly proportional to the FUNC OUT instantaneous value multiplied by the sum of the amplitude control voltage (VAMP) from the microprocessor board and the instantaneous value of the external amplitude modulation signal at AM In.

Refer to simplified schematic figure 4-12. All circled numbers are U31 pin numbers. When the instantaneous values of VAMP and AM In are equal, the base voltages of Q1 and Q2 are the same and 8mA flows through the 1.21kΩ resistor R213. This current is evenly split through diodes CR1 and CR2, Q1 and Q2, Q3 and Q4. Because the bases of Q3 and Q4, and the anode of CR3 are common to each other, and each have 500Ω resistors which are also commonly connected, the same amount of current (4mA) must flow through each of the three legs.

If VAMP does not equal AM In, current flows through the gain resistors R222 and R232 causing the currents in Q1 and Q2 become unequal. The direction of this current flow, and therefore the change in current through Q1 and Q2, depends on the polarity of the unequal inputs.

With 0 volts present at FUNC OUT, U31 pins 10 and 11 are at − 0.7V, and R205 has no current through it. Note that the total resistance of R3 and R219 (2500 Ω) is twice that of R4 and R206 (1250 Ω). Because these components are across the same voltage points, twice the current (8mA) flows through R4 and R206 as through R3 and R219. Also note that the bases of Q11, Q12 and the anode of CR4 are all common to each other, each with 500Ω resistors which are also commonly connected. The voltage and therefore the current (8mA) are identical for each of these three legs. Currents entering the collectors of Q11 and Q12 are equal under all conditions, and collector currents of Q9 and Q10 are also equal when Func Out is 0V. This means that the net emitter currents of both differential pairs (Q5/Q6 and Q7/Q8) are equal. Because of the cross connection of collector currents, the currents entering the multiplier at pins 2 and 14 are equal whether or not pins 9 and 12 have equal base voltages. When Func Out is not zero, R205 redistributes the Q9 and Q10 emitter currents to maintain equal currents through Q11 and Q12 collectors. Only when there is an instantaneous difference between VAMP and

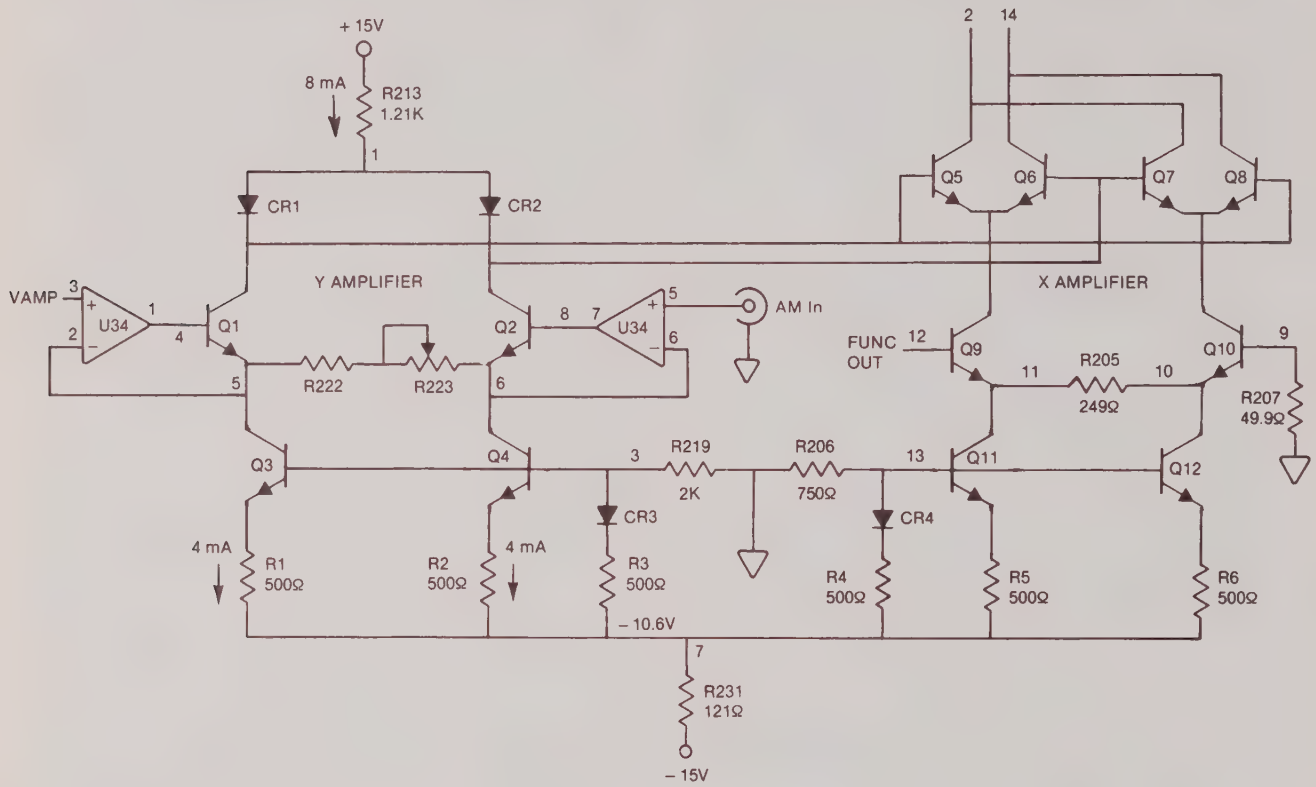


Figure 4-12. XY Multiplier Simplified Schematic

AM In and at the same instant Func Out is non-Zero is there a difference between the currents in pins 2 and 14. This difference is detected differentially and amplified by the power amplifier. In this manner, 4 quadrant multiplication is achieved. Func Out carrier amplitude is determined by the instantaneous difference of the dc value VAMP and AM In. Removal of VAMP with modulation at AM In produces SCM.

4.11.7 Output Amplifier

The output amplifier (ref. schematic 0103-00-1455 sheet 5) provides the final gain and output drive capabilities of the instrument. Differential currents from the XY multiplier are sensed by Q49 and detected at the + and – inputs of U33. Depending on the status of these currents, U33 pins 11 and 6 regulate the power supply currents through R244 and R256, and therefore the voltages at the bases of Q51 and Q53. These transistors drive the output complimentary emitter followers Q52 and Q54. The output voltage is fed back through R238 with the ratio of voltage divider R236 and R238 (between the output point and ground) determining the voltage at the output of U33 pin 10.

When pins 2 and 14 of the XY multiplier IC, U31 sink equal currents, the voltages at U33 pins 4 and 5 are equal, preventing the output of U33 at pin 10 from either sinking or sourcing current. In this condition, the power supply requirements of U33, sensed by the drops in R244 and R256 are static, causing Q51 to source and Q53 to sink idling current through CR49 and CR51. This idling current is mirrored by Q52 and Q54 by holding the V_{BE} of both transistors equal to the diode drops. In this manner, cross-over distortion, which is normally seen as the output voltage passes through 0V, is eliminated in this complimentary emitter follower.

When the XY multiplier IC U31 pin 2 sinks less current than pin 14, the voltage across R235 decreases while the voltage across R234 increases. This raises the the emitter voltage of the right hand transistor of Q49 while

lowering the emitter voltage of the left hand transistor. The right side of Q49 now sinks more current and the left side of Q49 sinks less current, bringing the "+" input of U33 higher than the "−" input. The output voltage at U33 pin 10 begins to rise, causing U33 to begin drawing more positive supply current through pin 11 than negative supply current through pin 6. This difference in supply current causes Q51 to source more than Q53 sinks and the PA OUT voltage will rise positive until the current through the feedback/divider resistors R238 and R236 provides the voltage needed at U33 pin 10 to stabilize the output. When this occurs, the supply currents of U33 equalize and equilibrium is established.

When the XY multiplier IC U31 pin 2 sinks more current than pin 14, the opposite condition occurs, and the PA OUT voltage goes negative until the current through the feedback/divider resistors R238 and R236 provides the voltage needed at U33 pin 10 to again stabilize the output. Note that the output voltage swing of U33 is very low resulting in a wide bandwidth without slew rate limiting. Trim capacitor, C153, is used to adjust the amplifier high speed signal peaking.

An offset voltage input at VOFST is converted to current through R125 and R126. This current is proportional to the voltage and polarity of VOFST, entering the summing node at U33 pin 4 to provide dc control of the input current, and therefore the output voltage offset.

4.11.8 Output Attenuator

The output attenuator (ref: schematic 0103-00-1455 sheet 6) consists of two output relays, K1 and K2, that are controlled by logic lines A0 and A1 from the analog interface circuit on the microprocessor/synthesizer board. These lines are driven by Q3 and Q2 respectively.

The three possible combinations of operating states for the relays are:

1. 50Ω output impedance matching: 55Ω in parallel with 555Ω in parallel with 5000Ω. K1 and K2 energized ($\overline{A0}$, $\overline{A1}$ low).
2. 20 dB attenuation: 55Ω from Func Out connector to ground; 555Ω in parallel with 5000Ω from PA OUT to Func Out connector. K1 energized ($\overline{A0}$ low), K2 dropped out ($\overline{A1}$ high).
3. 40 dB attenuation: 55Ω in parallel with 555Ω from Func Out connector to ground; 5000Ω from PA OUT to Func Out connector. K1 and K2 dropped out ($\overline{A0}$, $\overline{A1}$ high).

Transient Suppression: Func Out connector transients are suppressed during power on and power off by applying −40dB of attenuation between PA OUT and the Func Out connector.

During power on or power off, $\overline{MR}$ is low, turning Q1 (on the microprocessor/synthesizer board) off. This opens the current path through the relays and Q1 and Q2. Thus K1 and K2 are dropped out (40dB attenuation) regardless of what A0 and A1 are doing. Once power has stabilized and $\overline{MR}$ goes high, Q1 and Q2 are enabled by $\overline{ON}$. A0 and A1 can then be used to program the attenuator.

Output Protection: There are two safeguards to protect the attenuator and output amplifier circuits against major damage due to accidental connection of external voltages, including line power, to the Func Out connector. These safeguards are:

1. Diodes CR50 and CR52 prevent the voltage at PA OUT from exceeding ±15V.
2. A fast-acting fuse (F3) is connected directly to the Func Out center conductor to guard against accidental application of up to 250 Vac or 350 Vdc. Diodes CR53 through CR52 conduct current to ground through the fuse whenever the instantaneous voltage at J23 exceeds ±12.7V.

4.12 SYNC OUT DRIVERS

The sync out drivers section provides sync outputs at TTL and ECL levels. A TTL to ECL conversion circuit taps the TTL signal to provide an ECL output. Both TTL and ECL circuits are protected by fast-blowing fuses at the center conductors of the connectors.

The TTL and ECL outputs are driven by the SYNC signal from the microprocessor/synthesizer board. This signal is selected by the frequency synthesizer from three sources, the waveform synthesizer, function generator and frequency synthesizer. The SYNC signal is buffered by U15 before reaching the TTL OUT connector. Diodes CR62 and CR63 prevent an accidentally applied external voltage from damaging U15 and the associated circuitry. If an excessive voltage is applied to the connector, the fast-blow fuse, F1, will open.

The ECL signal is derived from the TTL signal and converted by the TTL to ECL circuit which includes Q38, Q39, Q40 and Q41. The voltage divider consisting of R170, CR35, CR36 and R171 maintains the base of Q39 at a predetermined level, and the collector provides a constant current to the emitters of differential amplifier transistors Q38 and Q41. The base of Q41 is set to +1.4V by divider R178, CR38 and CR37. Diode CR39 is forward biased and maintains the Q40 base voltage 0.7V more positive than the switching signal at the collector of Q41. This voltage change is nullified across the base emitter junction of emitter follower and output drive transistor Q40, making the voltage at the collector of Q41 equal to the collector of Q40. As with the TTL circuit, diodes CR59 and CR60 prevent an accidentally applied external

voltage from damaging Q40 and the associated circuitry. If an excessive voltage is applied to the connector, the fast-blow fuse, F2, will open.

4.13 POWER SUPPLY

Three power supply voltages, +15V, −15V, and +5V are generated on the power supply circuit board (ref: schematic 0103-00-1113).

4.13.1 ±15V Power Supplies

The ±15V Power Supplies provide power to the analog sections of the instrument. Voltage regulator VR1 maintains the 15 volt supplies within ±0.3V. The pass elements, Q1 and Q2, provide greater output current than is possible with only the regulator. R2, which is in series with the output of the +15V regulator, causes current limiting to take place at a lower value than the internal limiting provided by the regulator. As the current through R2 (located between the regulator output and reference pins) reaches its limiting value, the voltage drop across R2 reaches 0.4V. Any further current through R2 causes the regulator to lower the output voltage until the current falls back to the limiting value.

The −15V supply operates similarly to the +15V supply, however the polarities are reversed.

4.13.2 +5V Supply

In the +5V supply, ac from the transformer, T1 (located on the rear panel), is rectified by CR2 and filtered by C9, C10, and C11 to provide unregulated dc for regulator VR2. C12 provides additional filtering at the output of the regulator.

4.13.3 Power Distribution

The microprocessor/synthesizer board primarily uses +5V for most of its circuits, however, ±15V is also needed for the frequency synthesizer. Power enters the board at the J4 POWER CONNECTOR. Each line is filtered by ferrite bead inductors FB2-FB4 and capacitors C21-C26. Additional filtering is provided by small value bypass capacitors at various locations on the board.

The waveform generator board needs ±15V for most of its circuits, however +5V is used in the various digital circuits, primarily in the waveform synthesizer and square selector. Power enters the board at the J5 POWER CONNECTOR. Filtering is provided by small value bypass capacitors at various locations on the board.

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize the turnaround time.

5.2 REQUIRED TEST EQUIPMENT

The test equipment required to perform the calibration procedures in table 5-2 are listed in table 5-1.

5.3 CALIBRATION

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

Disconnect the instrument from the ac power source, then slide both top and bottom covers **partially** off (see figure 2-1, paragraph 2.2.2). Remove only the **top** cover, slide the bottom cover back on, and invert the instrument to maintain the operating temperature during calibration.

Reconnect the instrument to the ac power source and allow it to warm up at least 30 minutes for final calibration. Slide the bottom cover toward the rear only when making adjustments or measurements.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of this manual.

Figure 5-1 shows waveform generator calibration points. Figure 5-2 shows microprocessor/synthesizer board calibration points.

Table 5-1. Required Test Equipment

Equipment	Quantity	Specifications
Oscilloscope	1	Dual channel, ⩾ 20 MHz bandwidth, external trigger input.
Frequency Counter	1	6½ digit resolution and period measurement capability.
True RMS Digital Voltmeter (DVM)	1	4½ digit resolution.
Distortion Analyzer	1	To 200kHz
Spectrum Analyzer	1	To 50MHz
Signal Source	1	Capable of 1 kHz, 10 Vp-p sine wave.
X1 Probe	1	
X10 Probe	1	
50Ω Termination	1	Feedthrough, 0.1% accuracy, 2W.
Coaxial Cables	3	BNC male connectors, RG-58U cable.
BNC Tee	1	1 male to 2 female connection.

Table 5-2. Calibration Procedure

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
1	Power Supply Regulators	DVM	J15 Pin 2	Reset		+ 5V ± 250mV	Ground lead to CR14 cathode
2			J15 Pin 7			− 15V ± 250mV	
3			J15 Pin 14			+ 15V ± 250mV	
4	Crystal Frequency	Counter	TTL Out	Mode: Clock Frequency: 10.000MHz	C29 Micro-processor/synthesizer board	10.000MHz ± 100Hz	Verify frequency resolution from 10 MHz to 32 MHz

In the following step, if necessary, preadjust R86 so that the phase lock loop output can be displayed on scope at 0.1V/div with roughly 0V dc offset. Adjust R184 to null the signal, then adjust slightly so that all phase correction pulses just begin pulsing in the positive direction.

5	Phase Lock Loop	Scope	J15 Pin 4	Mode: Synth Frequency: 1.000kHz	R86 R184	See above	Use X10 probe (Ground lead to CR14 cathode)
6	LF Waveform Check		Func Out (Terminated into 50Ω or 75Ωif Opt 003 installed or 600Ω if Opt 004 installed)	Reset Frequency: 999Hz Amplitude: 10.2Vp-p		Verify all LF waveform functions, then return to sine.	
7	Carrier Null			Press "Amplitude" Press "Zero"	R204 R214	Minimum AC signal	Scope settings: 10mV/div. 0.5msec/div AC coupled input
8	Modulation Null			Press "Amplitude" Function: DC	R147		Scope settings: 5mV/div. DC coupled input Sync to 1kHz 10Vp-p sine applied to Ext AM In
9	"0" AM Null	DVM		Function: Sine Press "Amplitude" Press "Zero"	R251	0Vdc ± 10mV	Disconnect Ext AM In
10	Maximum Amplitude Null			Press "Amplitude"	R247		
11	Worst Case Offset			Amplitude: Value between 1 and 10.2Vp-p producing greatest offset from 0Vdc			Record value and polarity
12	Worst Case Offset Adjustment				R203	Double Above recorded value (same polarity)	

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
13	Amplitude Null			Amplitude: 10.2Vp-p	R247	0Vdc ± 10mV	
Repeat steps 9, 11, 12 and 13 until offset values are all within 10mV of 0Vdc from 1 to 10.2Vp-p.							
14	SCM Balance	Scope		Press "Zero"	Only if necessary, adjust R147 (waveform top) SCM NULL with front knob (waveform bottom)	Equal amplitude alternate peaks	Scope settings: 1/div. 5msec/div. Sync to 50Hz 10Vp-p sine applied to Ext AM In Return SCM NULL to 000 after R147 set.
15	AM Check			Amplitude 5Vp-p		≈100% modulated AM waveform	Disconnect Ext AM In signal until amplitude and scope set. Scope setting: 2V/div.
16	VCG Zero	DVM (low DC range, no load)	VCG In	Function: Square Amplitude: 10.2Vp-p Frequency: 9.99kHz Press "Zero"	R96	0Vdc ± 0.1mV	Disconnect applied signal from Ext AM In and scope.
17	1000:1 Frequency	Scope	Func Out (Terminated into 50Ω, or 75Ω if Opt 003 installed or 600Ω if Opt 004 installed)		R70	Negative to positive transition at 5.5cm	Disconnect cable from VCG In Scope settings: 10msec/Div., Trig Mode Normal, DC, Negative Slope
18	1000:1 Symmetry				R73	<1% assymmetry	Scope setting: Magnify X10 On
Repeat steps 17 and 18 as needed.							
19	Symmetry			Press "Frequency" Frequency: 5.00 kHz	R88	<0.1% assymmetry	Scope Settings: 20μsec/div. Magnify X10 On (or X100 if possible)
20	Sine Dist	Distortion analyzer		Function: Sine	R100, R105, R106, R113	Minimum distortion (typically 0.1 to 0.2%)	Scope Setting: Magnify X10 Off

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
21	Frequency Ranges	Counter	TTL Out (Terminated into 50Ω)	Function: Square Frequency: 99.9kHz	R86	99.9kHz ± 1kHz	
				Frequency: 9.99kHz	C28 (Trim)	9.99kHz ± 100Hz	
				Frequency: 1MHz	C37, C25 (Trim)	1MHz ± 10kHz	
				Frequency: 999kHz	C38, C26 (Trim)	999kHz ± 10kHz	
				Frequency: 12.00MHz	R66	12.00MHz ± 100kHz	
Repeat 1MHz, 999kHz and 12.00MHz adjustments as needed.							
22	Sine Amplitude	DVM (True RMS)	Func Out (Terminated into 50Ω, or 75Ω if Opt 003 installed or 600Ω if Opt 004 installed)	Function: Sine Frequency: 1.00kHz	R223	3.606 Vrms ± 10mV	
23	LF Amplitude			Frequency: 999Hz	R2		
24	DC Output			Function: DC Offset: +5.1V and −5.1V alternately	R125 (gain) R251 (offset)	±5.1Vdc ± 10mV	
25	Sine Offset			Offset: "Zero" Function: Sine	R247	0Vdc ± 10mV	
26				Frequency: 1.00kHz	R107		
27	Triangle Offset			Function: Triangle	R166		
28	Triangle Amplitude				R161	2.944Vrms ± 10mV	
29	Square Amplitude/ Offset			Function: Square	R117 (Upper) R118 (Lower)	5.100Vrms ± 10mV 0Vdc ± 10mV	DVM t DC. Remove half error with R117, half with R118. DVM to Vrms. Remove half error with R117, half with R118.
Repeat Step 29 until both amplitude and offset errors are <10mV.							

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
30	Trigger Baseline			Mode: Triggered Function: Triangle Frequency: 9.99 kHz	R26	0Vdc ± 20mV	
31	Rise/Fall Time	Scope		Mode: Continuous Frequency: 1.00MHz Function: Square	R232, R258, C153	Rise/Fall Time ⩽22ns (50/75Ω machines) Best response on 600Ω machines	Use 50Ω termination regardless of option. Scope Settings: 0.1μs/Div. Set waveform for 0% and 100% lines on Scope Magnify X10 On
32	Aberrations					Peak-to-Peak aberrations <400mV	Magnify X10 Off
33	Harmonics	Spectrum Analyzer	Func Out (Use X10 attenuator for 50 and 75Ω machines. All machines not terminated)	Function: Sine		All harmonics at least −28dBc from 1MHz to 12MHz	
			Repeat steps 31, 32 and 33 as needed.				
34	Post-Final checks Repeat steps 4, 9, 16, 17, 18, 22-29	See each step	See each step	See each step	See each step	See each step	Install both covers, then set instrument aside for 1 hour with power on to stabilize. Rapidly check indicated steps and touch-up adjustments as needed.

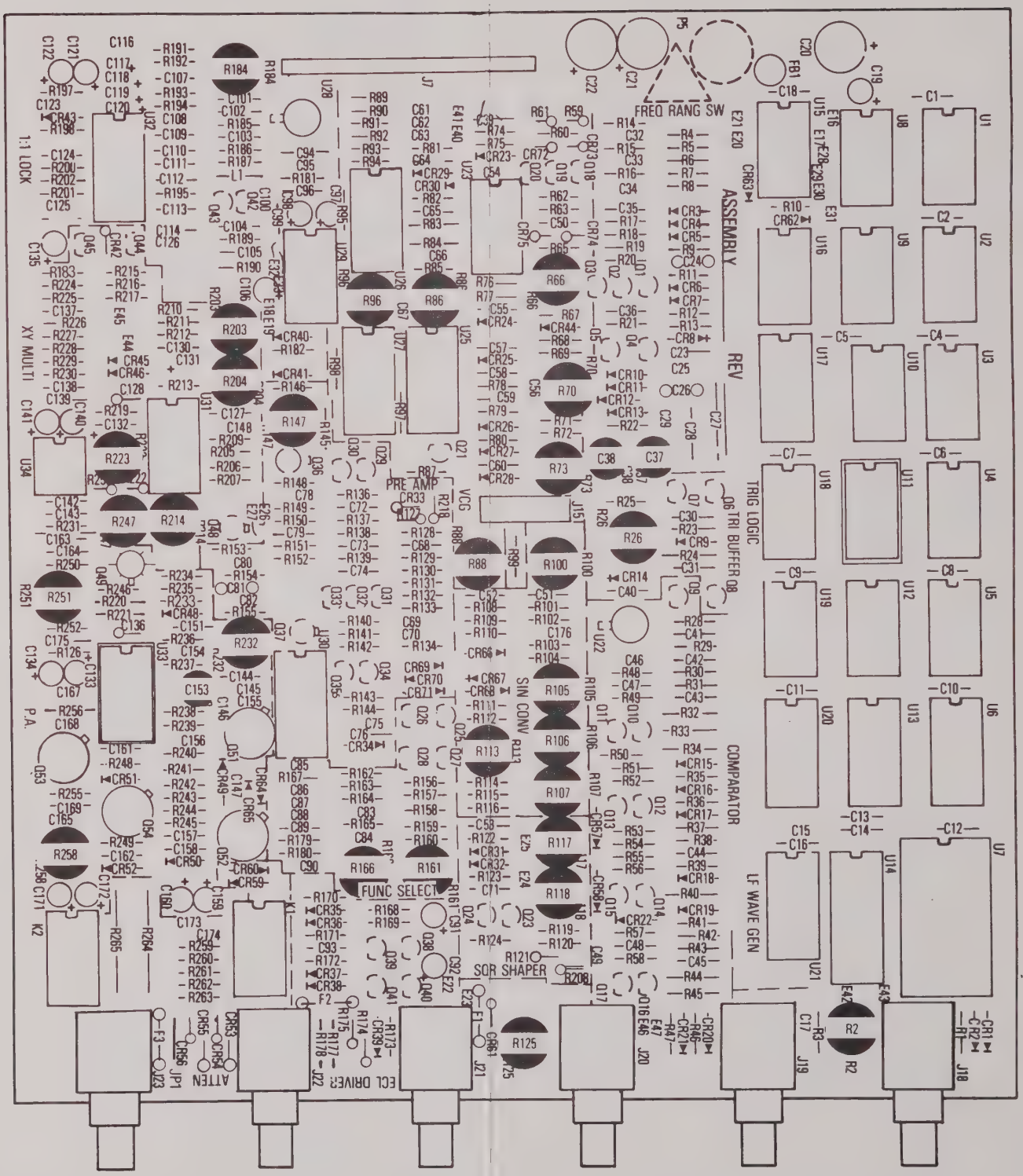


Figure 5-1. Waveform Generator Board Calibration Points

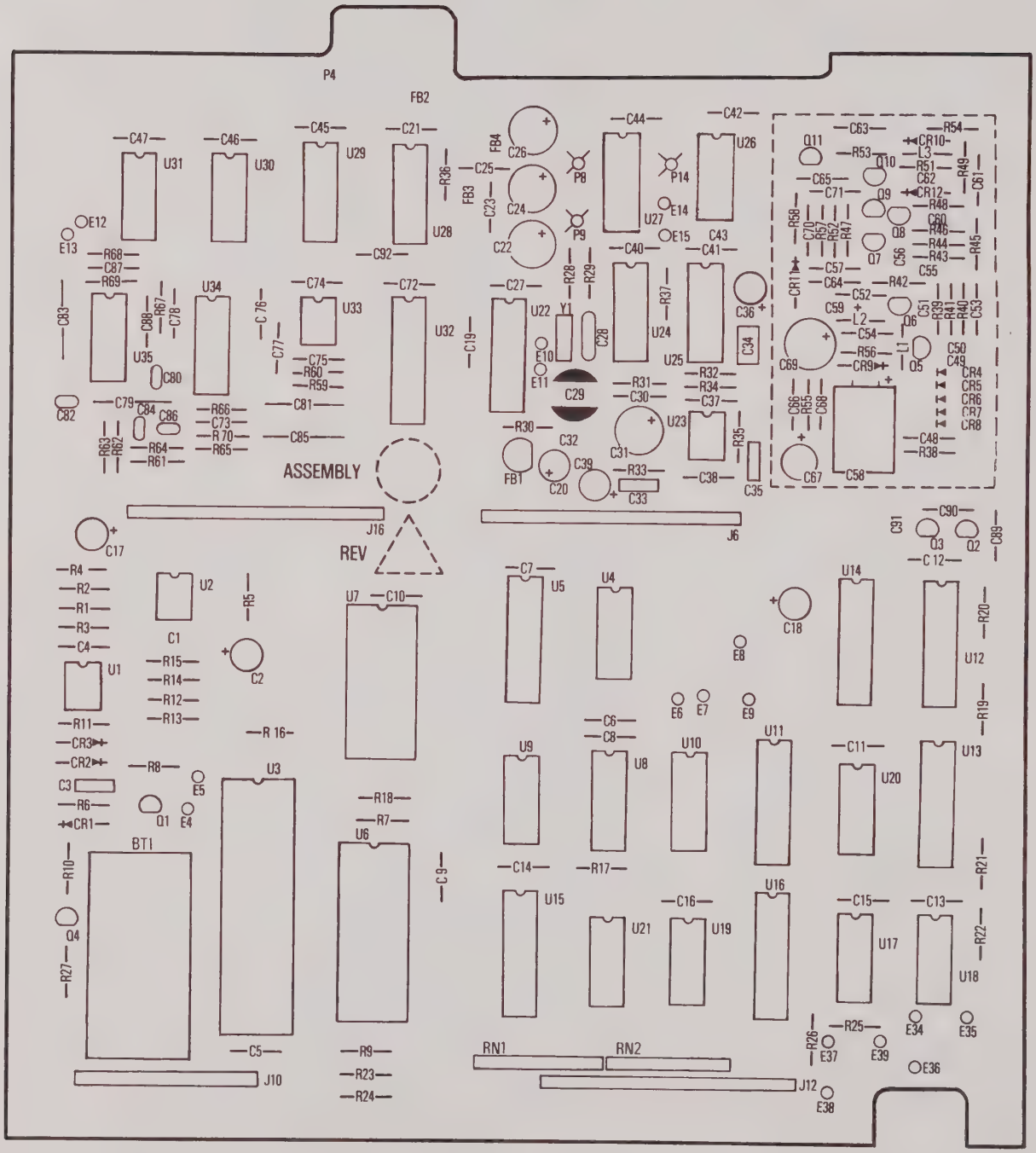


Figure 5-2. Microprocessor/Synthesizer Board Calibration Points

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description (Section 4) in conjunction with the schematics (Section 7). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

The intent of this section is to provide the information required to return this instrument to proper operation. Information is divided into two parts. Part one (table 6-1) contains a list of symptoms that should be useful in determining which circuit within the instrument is defective. Part two consists of circuit guides which include settings and measurements for troubleshooting an individual block. Each circuit guide also references related schematics, circuit descriptions, and calibration procedures. Table 6-2 provides a list of these circuit guides.

Before beginning the troubleshooting process, verify the instrument's controls are set correctly. For example, the instrument cannot produce a 100kHz ramp up. For more information about instrument operation, refer to section 3 of this manual.

Also, rule out calibration as a possible problem. For instance, if the 10 kHz triangle amplitude is out of specification while the sine and square amplitudes are in specification, then the TRI LEVEL pot, R161, quite possibly, needs adjustment.

Finally, inspect the instrument's components, wiring, and circuit boards for heat damage.

6.2.1 Isolating a Problem

To successfully troubleshoot this instrument, the symptom must first be identified, the faulty block isolated, the block analyzed, and the defective component located and replaced.

To identify the symptom, use all the front panel controls and connectors. Pay particular attention to the frequency range, as this identifies the signal flow (function generator loop or waveform synthesizer).

Once the signal flow is established, table 6-1 can be used to isolate the circuit block. Start measuring the outputs of the circuit blocks until the defective block is located.

Once the block is isolated, refer to the appropriate circuit guide (table 6-2). Set the controls as instructed and take the measurements given to check out the block. Paragraph 6.3.45 gives component troubleshooting information.

When the microprocessor and interface system is suspect, troubleshooting can be done by observing the symptoms to decide which checks will be used to locate a faulty digital circuit block. General techniques of troubleshooting digital systems are then applied to these blocks. One valuable technique involves using an oscilloscope to check for "stuck" bits on each line of a constantly varying address or data bus. A "stuck" bit may be constantly high, low, or tri-state (the output floats to a threshold level of 2 to 2.5V). It could also vary between a tri-state and a high or a low level without going to the third level. The cause of a "stuck bit" can be found by isolating IC pins and connectors from the line in question. If more than one line is "stuck", make a list of these lines and check for a common IC.

Table 6-1. Fault Isolation

Symptom	Possible Cause or Refer to Paragraph
Display blank, power supplies normal.	Display view angle misadjusted. Paragraph 6.3.17
Fuse blows, display blank.	Paragraph 6.3.44.
Power supply out of specification.	Paragraph 6.3.44.
Func Out (all functions) distorted or missing (TTL/ ECL outputs and display normal).	Paragraphs 6.3.38 to 6.3.41.
TTL Out missing, ECL, Func Out and display normal.	Fuse F1
ECL Out distorted or missing, TTL, Func Out and display normal.	Paragraph 6.3.43.
TTL and ECL outputs distorted or missing, Func Out and display normal.	Paragraphs 6.3.30 and 6.3.42
All outputs (all functions) distorted or missing above 1 kHz, display normal.	Paragraphs 6.3.8, 6.3.7, 6.3.12 and 6.3.20 to 6.3.29.
All outputs distorted or missing at 1 kHz or lower frequency, display normal.	Paragraphs 6.3.32
Square output distorted or missing (remaining waveforms and display normal).	Paragraphs 6.3.36 and 6.3.37
Sine wave or triangle outputs distorted or missing (remaining waveforms and display normal).	Paragraph 6.3.34 and 6.3.35
High frequency distortion or frequency problems at Func Out. Display and remaining outputs normal.	Paragraph 6.3.28
Time symmetry cannot be adjusted within specification.	Paragraphs 6.3.20 and 6.3.21
Trigger, gate and trigger baseline problems.	Paragraphs 6.3.22 and 6.3.29
Voltage at VCG IN connector not changing frequency properly.	Paragraph 6.3.20
DC offset not functioning correctly.	Paragraphs 6.3.12 and 6.3.39
Display blank or shows unintelligible data (not reading "WAVETEK MODEL 23" or "WAVETEK MODEL 23 * BATTERY LOW! *")	J15 pins 2, 7 or 14. Paragraphs 6.3.1, 6.3.2 and 6.3.17.
Display reads "WAVETEK MODEL 23 * BATTERY LOW! *" or "WAVETEK MODEL 23" followed by data not related to the turn-off setup.	Battery Paragraph 6.3.15.
Memory retained but battery life much less than specified.	Paragraph 6.3.14.
Not frequency synthesizing properly.	Paragraphs 6.3.30 and 6.3.31

6.3 TROUBLESHOOTING GUIDES

Table 6-2. Circuit Block Guides

Circuit Guide	Paragraph
Microprocessor	6.3.1
Clock	6.3.2
Front Panel Interface	6.3.3
Address Latch	6.3.4
ROM	6.3.5
RAM	6.3.6
Data Latch	6.3.7
Analog Interface	6.3.8
Knob Interrupt	6.3.9
Analog/Panel Decoder	6.3.10
Address Decoder	6.3.11
Sample and Hold	6.3.12
Reset	6.3.13
Standby	6.3.14
Battery Test	6.3.15
Keyboard	6.3.16
Display	6.3.17
GPIB	6.3.18
RS-232	6.3.19
VCG	6.3.20
Current Source and Sink	6.3.21
Trigger Control Current Sink	6.3.22
Current Switch	6.3.23
Frequency Range Switches	6.3.24
Triangle Buffer	6.3.25
Comparator, Switch and	6.3.26
Square Buffers	6.3.27
High Frequency Compensation	6.3.28
Trigger Logic	6.3.29
Frequency Synthesizer	6.3.30
1:1 Lock Loop	6.3.31
Waveform Synthesizer	6.3.32
Sine Converter	6.3.33
Function Selector	6.3.34
Preamplifier	6.3.35
Square Selector	6.3.36

Table 6-2. Circuit Block Guides (Continued)

Circuit Guide	Paragraph
Square Shaper	6.3.37
XY Multiplier	6.3.38
Power Amplifier	6.3.39
Attenuator	6.3.40
Output Protection	6.3.41
TTL Driver	6.3.42
ECL Driver	6.3.43
Power Supply	6.3.44

6.3.1 Microprocessor

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.1.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-3 to fault isolate the microprocessor and associated circuitry.

6.3.2 Clock

Related information in this manual.
Schematic: 013-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.2.

Refer to table 6-4 to fault isolate the clock and associated circuitry.

6.3.3 Front Panel Interface

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.3

Check U15 pin 1 and U16 pin 1 (increase scope intensity) for negative pulses ≅0.5μs wide occurring at 33ms intervals. If readings are not normal, refer to the analog panel decoder (paragraph 6.3.10).

Refer to table 6-5 to fault isolate the front panel interface input lines and associated circuitry.

Table 6-3. Microprocessor Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U3 pin 3	3.072MHz	Clock (paragraph 6.3.2)
U3 pin 39	768kHz positive TTL pulse	U3, U5 or associated circuitry
U3 pin 40	768kHz TTL square wave	U3 or associated circuitry
U3 pin 21	≅ + 4.5V	CR2 or power supply (paragraph 6.3.44).
U3 pin 6	TTL high.	Reset circuitry (paragraph 6.3.13).
U3 pin 7	TTL high.	Standby circuitry (paragraph 6.3.14).
U3 pin 5	TTL High. Pulses low when rotating knob.	Knob Interrupt (paragraph 6.3.9).
U3 pins 22 through 37	TTL high with groups of pulses occurring for ≅1ms at intervals of 16.5ms.	"Stuck" bits at U3 or associated circuitry. U6 (paragraph 6.3.5).
The remaining U3 pins are discussed in the appropriate troubleshooting paragraphs.		

Table 6-4. Clock Signal Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading	Remarks
U22 pin 15	6.144 MHz roughly triangular waveform at TTL level.	Y1, U22, U4, E10 to E8 coax	Remove ribbon cable from J6 for access to U22 pins.
U4 pin 11		E10 to E8 coax	
U4 pin 9	3.072 MHz TTL signal.	U4, U3, E6 to E4 coax	Reconnect ribbon cable after fault is corrected.
U3 pin 3		E6 to E4 coax	

Table 6-5. Front Panel Interface Input Fault Isolation

Observe a high to low transition when the indicated key is pressed. If any signal is bad, go to paragraph 6.3.16.

Pin	Key	Pin	Key
U15 pin 2	RESET	U16 pin 2	KNOB*
U15 pin 4	TRIGGER	U16 pin 6	KNOB*
U15 pin 6	SLOPE	U16 pin 11	AMPLITUDE
U15 pin 8	ZERO	U16 pin 13	MODE/FUNC
U15 pin 11	<	U16 pin 15	OFFSET
U15 pin 13	>	U16 pin 17	KNOB
U15 pin 15	STATUS		
U15 pin 17	FREQ/PER		

*May be high or low after rotation.

Check U3 pins 30 through 37 (AD0-7) for a "stuck" bit. If not normal, isolate and replace appropriate IC.

6.3.4 Address Latch

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.4.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-6 to fault isolate the address latch and associated circuitry.

Table 6-6. Address Latch Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U5 pin 11	768kHz positive TTL pulse	U3 (paragraph 6.3.1), U5 (paragraph 6.3.4) or associated circuitry
U5 pins 2 through 9 and 12 through 19	Varying Lines at TTL Levels	IC causing a "stuck" bit.

6.3.5 ROM

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.5.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-7 to fault isolate the ROM and associated circuitry.

Table 6-7. ROM Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U6 pin 20	Positive pulse groups at 16ms intervals	If active but not normal, U3 (paragraph 6.3.1), U6/U7 (paragraph 6.3.6) If not active, U8/U21 (paragraph 6.3.11).
U6 pin 22	Similar to 768kHz square E clock (frequency may appear lower on counter) with a few missing pulses	U3 (paragraph 6.3.1), U6, U18 or U20
U6 pins 2 through 13, 15 through 19, 21, and 23 through 26	Varying Lines at TTL levels	U3 (paragraph 6.3.1) or any IC connected to suspect line

(Even if all bits are functional U3, U6 or U7 may be at fault)

Table 6-8. RAM Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U7 pin 18	Negative pulse groups at 16ms intervals	If active but not normal, U3 (paragraph 6.31.), U6 (paragraph 6.3.5) or U7 If not active, U8/U9 (paragraph 6.3.11)
U7 pin 24	≅ +4.5V.	CR2 or power supply (paragraph 6.3.44)
U7 pin 20	Similar to 768k square E clock (frequency may appear lower on a counter) with a few missing pulses	U3 (paragraph 6.3.1), U6 (paragraph 6.3.5), U18 or U20
U7 pin 21	Negative pulses	U3 (paragraph 6.3.1), U19, U20 or U7
U6 pins 2 through 13, 15 through 19, 21, and 23 through 26	Varying Lines at TTL levels	U3 (paragraph 6.3.1) or any IC connected to suspect line
(Even if all bits are functional U3, U6 or U7 may be at fault)		

6.3.6 RAM

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.6.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-8 to fault isolate the RAM and associated circuitry.

6.3.7 Data Latch

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.7.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-9 to fault isolate the data latch and associated circuitry.

Table 6-9. Data Latch Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U11 pin 11	768kHz square (E clock)	U3 (paragraph 6.3.1).
U11 pins 3, 4, 7, 8, 13, 14, 17 and 18	Varying lines at TTL levels	U11, U3 (paragraph 6.3.1) or any IC connected to suspect line causing a "stuck" bit.
(Even if all bits are functional U3, U6 or U7 may be at fault)		
U11 pins 2, 5, 6, 9, 12, 15, 16 and 19	Varying lines at TTL levels	U11, U12, U13, U14 or U32

Table 6-10. Knob Interrupt Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
Display	Responds to keystrokes	U3 (paragraph 6.3.1), U6 (paragraph 6.3.5), U7 (paragraph 6.3.6).
U18 pins 2 and 5	Activity while knob is rotated	Keyboard (paragraph 6.3.16)
U17 pin 1 (RKIRQ)	Activity while knob is rotated	U10 (paragraph 6.3.10) if RKIRQ missing but KW1, KW2 and KM normal.
U3 pins 5 and 15	Negative and positive pulses respectively as knob is rotated	Knob interrupt circuit (U17, U18, U19 and Q4

6.3.8 Analog Interface

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.8.

Verify paragraphs 6.3.10 and 6.3.1. Return here if normal.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Check U11 pins 2, 5, 6, 9, 12, 15, 16 and 19 for varying lines at TTL levels. If readings are not normal, problem could be on the waveform generator board, or an IC such as U11, U12, U13, U14 or U32 on the microprocessor/synthesizer board. The boards can be separated by disconnecting J6.

6.3.9 Knob Interrupt

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.9.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-10 to fault isolate the knob interrupt and associated circuitry.

6.3.10 Analog/Panel Decoder

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.10.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-11 to fault isolate the analog/panel decoder and associated circuitry.

Table 6-11. Analog/Panel Decoder Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U10 pin 6	768kHz square wave	U3 (paragraph 6.3.1), U10, U18.
U10 pins 1, 2 and 3	Groups of negative pulses at 16ms intervals	U3 (paragraph 6.3.1)
U10 pin 4	Groups of positive pulses at 16ms intervals	U3 (paragraph 6.3.1)

Table 6-11. Analog/Panel Decoder Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U10 pin 5	Groups of negative pulses at 16ms intervals	U10 or U8 (paragraph 6.3.11)
U10 pin 7	≅ 0.5μs negative pulses (with (with increased scope intensity) as knob rotated	U3 (paragraph 6.3.1), knob interrupt logic (paragraph 6.3.9), or U10.
U10 pins 9 and 10	≅ 0.5μss pulses at 33ms intervals (with increased scope intensity)	U10, U15 or U16 (paragraph 6.3.3)
U10 pins 13, 14 and 15	≅ 0.5μs negative pulses as knob rotated	U10, U12, U13 or U14 (paragraph 6.3.8)

6.3.11 Address Decoder

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.11.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-12 to fault isolate the address decoder and associated circuitry.

Table 6-12. Address Decoder Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U8 pins 1, 2 and 3	Negative pulses at ≅ 16ms intervals	If pins 1, 2 and 3 are continuous (not pulsing), pin 7 pulses positive, and pins 9 and 12 pulse negative, U8 is functional.
U6 pin 20	Positive pulses	U6 or U21
U9 pin 2 and U8 pin 12	Identical readings	U9 if MR/ low (see paragraph 6.3.13) and U9 pin 14 has ≅ +4.5V. If pins 1, 2 and 3 are continuous (not pulsing) and pin 7, 9 and 12 are not active, replace U8. Check paragraphs 6.3.1, 6.3.5 and 6.3.6.
U19 pin 1 Set scope for normal triggering, negative slope, high intensity.	≅ 0.5μs negative pulses as as knob rotated after pressing Frequency/Period button	U8, U19, or U22
U19 pin 2 Change scope setting to positive slope.	≅ 0.5μs positive pulses as knob rotated after pressing Frequency/Period button	U8, U19, or U22

Table 6-12. Address Decoder Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U8 pin 11	Negative pulses at 33ms intervals	U8 or U33
U8 pin 13	TTL high. Pulses low after interface option interrupts microprocessor.	U8. See also paragraph 6.3.18 and 6.3.19.
U8 pin 14	TTL high. Pulses low when knob rotated.	U8 or U19
U8 pin 15	Negative pulses at 16ms intervals.	U8 or U10

6.3.12 Sample and Hold

Related information in this manual.
Schematic: 0103-00-1454 Sheet 2.
Circuit Description: Paragraph 4.2.12.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-13 to fault isolate the sample/hold and associated circuitry.

Table 6-13 Sample and Hold Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U32 pin 2	768kHz square wave	U3 (paragraph 6.3.1).
U32 pin 3	Negative pulse groups at 16ms intervals.	U3 (paragraph 6.3.1).
U32 pin 1	Negative pulses at 33ms intervals.	Address decoder (paragraph 6.3.11).
J15 pins 7 and 14 on the generator board	±15V power supplies.	Power supply (paragraph 6.3.44).
U32 pin 13	≅ −10.2Vdc.	U33A circuitry or U32
U32 pin 12	0Vdc	U32, U33B circuitry or a LAD0-7 "stuck" bit.
U32 pin 14	Following a reset, ≅ +5Vdc with negative pulses at 33ms intervals. Pulses vary with knob.	U32, U33B circuitry or a LAD0-7 "stuck" bit.

Table 6-13. Sample and Hold Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U34 pins 1, 8, 9 and 16	Negative pulses at 33ms intervals.	U3, U6, U7 or U34
U35 pin 1 (VAMP)	+1Vdc to +10Vdc as amplitude varied from 1Vp-p to 10Vp-p after pressing Reset, Amplitude.	U34 or U35
U35 pin 7 (VOFST)	−10Vdc to +10Vdc in a complex fashion as offset varied from −5.1V to +5.1V after setting amplitude to minimum and pressing Offset.	U34 or U35
U35 pin 8 (VFREQ)	+10Vdc to +1Vdc as frequency is varied from 9.99kHz to 1kHz after pressing RESET, Frequency.	U34 or U35
U35 pin 14 (VNULL)	0Vdc to −10Vdc as knob rotated ccw after pressing Amplitude, Zero. Increases to +10Vdc as knob rotated cw.	U34 or U35

6.3.13 Microprocessor Section Reset

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.13.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Press Reset on the instrument front panel.

Connect channel 1 probe to +5V supply at rear of R5 (near U2).
Connect channel 2 probe to front of R5.

Set controls as follows:

Vertical Mode: Chop
Trig Mode: P-P Auto during setup, Normal when taking readings
Trig Source: Channel 1
Trig Slope: Positive
Trigger level: Positive, displaying one trace each time the unit is powered On.
Horiz Sweep: 20ms/Div

Observe ≅ 130ms delay between channel 1 and channel 2 positive transitions as unit is powered On. If reading not normal, U2, U3, U9 or interface option board could be bad.

6.3.14 Standby

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.14.

Verify paragraph 6.3.13 normal before proceeding.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Connect channel 1 probe to left end of R3 (viewed from front of instrument).
Connect channel 2 probe to right end of R3 (viewed from front of instrument).

Table 6-14. Battery Test Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U3 pin 21, U7 pins 18 and 24, U9 pin 14, and across the battery	>+2.2Vdc (typically 2.8Vdc) with power Off. (All voltages must be present for memory retention).	U1B circuitry, U3, U7 or U9 or battery holder.
U3 pin 11	Battery voltage present with Power Off.	U1B circuitry.
U3 pin 11	Single momentarily low pulse, then constant battery voltage at Power On.	U1B circuitry.
5U3 pin 12	Low if battery voltage >2.2V.	U1B circuitry or U3.

Set controls as follows:

Vertical Mode: Chop
Trigger Source: Channel 1
Trig Mode: P-P Auto during setup, Normal when taking readings
Trig Slope: Negative
Trigger level: Positive, displaying one trace each time the unit is powered Off.
Horiz Sweep: .5ms/Div
Horizontal Position: Sweep begins at center of screen

Observe both points TTL high during setup. As the unit is powered Off and the level at channel 2 just starts to decay (about 1.5ms after power Off), channel 1 should make a high-to-low transition. If reading not normal, U1, U2 or U3 could be bad.

6.3.15 Battery Test

Related information in this manual.
Schematic: 0103-00-1454 Sheet 1.
Circuit Description: Paragraph 4.2.15.

Continue with this paragraph only if the battery has been replaced and the problem persists. A display of "WAVETEK MODEL 23 ** COLD START **" would be proper on the first power up after replacing the battery.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Refer to table 6-14 to fault isolate the battery test and associated circuitry.

6.3.16 Keyboard

Related information in this manual.
Schematic: 0103-00-1701 Sheet 1.
Circuit Description: Paragraph 4.3.1.

Perform paragraph 6.3.3 tests before proceeding.

Inspect connections between U15, U16 and J12. Remove front panel and keyboard by removing screws under bezel strip (Reset to Power keys) to inspect key targets for cleanliness and lack of corrosion and conductive rubber keystrip for alignment over key targets. Repair as needed.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

6.3.17 Display

Related information in this manual.
Schematic: 0103-00-1701.
Circuit Description: Paragraph 4.3.3.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Inspect connectors W5 and J10.

Refer to table 6-15 to fault isolate the display and associated circuitry.

Table 6-15. Display Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
J10 pins 1 and 2	0V and +5V respectively.	J10, power supply (paragraph 6.3.44) or display (paragraph 6.3.17).
J10 pin 3	≅ +2V when display view angle adjust set fully up. ≅ −1V when set fully down.	J10 or display (paragraph 6.3.17).
J10 pins 4, 5 and 7 through 14.	Negative pulse groups at 16ms intervals.	"Stuck" bits at U3 (paragraph 6.3.1) or associated circuitry
J10 pin 6	Pulses low to high when any key pressed.	U19, U21 or display module.
If readout bad but all display inputs good, replace display module.		

6.3.18 GPIB

Related information in this manual.
Schematic: 0103-00-1678 Sheet 1.
Circuit Description: Paragraph 4.4.1.

All components referenced in this paragraph are located on the option board unless otherwise specified.

Refer to tables 6-16 and 6-17 to fault isolate the GPIB and associated circuitry.

Refer to table 6-18 to fault isolate J16 (microprocessor/synthesizer board) and associated circuitry.

Table 6-16. GPIB Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
Front Panel (Rear panel Interface disconnected)	Proper local control	If abnormal operation with J16 (microprocessor/synthesizer board) disconnected, U3 (microprocessor/synthesizer board paragraph 6.3.1) or associated circuitry.
		If normal operation with J16 (microprocessor/synthesizer board) disconnected, check for a "stuck" bit at J16.
Display (Rear panel Interface disconnected)	"WAVETEK MODEL 23 OPT 001 IEEE-488" momentarily after cycling Power Off, then On.	U2 or incorrect signal on a J16 (microprocessor/synthesizer board) line. See table 6-18.
Display	Use Status and ◀ buttons to verify Address matches ADDRESS SELECTOR (SW1) setting	SW1, R1, U1 or U2.

Table 6-16. GPIB Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U2 pins 16, 17, 18, 25	High	U2, U3 or U4.
U2 pin 27	Low	U2, U3 or U4.
U2 pins 23, 26 and 29 through 36	Floating (tri-state)	U2, U3 or U4.

NOTE

Connect GPIB cable to rear panel for the following tests.

Table 6-17. Controller Assisted GPIB Fault Isolation

Program From Controller	Incorrect Reading	Possible Cause of Incorrect Reading
Send data to the Model 23's listen address in a continuous loop.	Bus error	U2 or U4.
	Incorrect data transmission (recall the command string).	U2 or U3, or W15 connections.
Request and display data in a continuous loop from the Model 23's talk address.	Bus error	U2 or U4.
	Incorrect data	U2 or U3.

Table 6-18. J16 (Microprocessor/Synthesizer Board) Signals

Test Point	Normal Reading	Possible Cause of Wrong Reading
J16 pin 1	Ground	J16 connector
J16 pin 2	+5V	J16 connector
J16 pin 3	+15V	J16 connector
J16 pin 4	−15V	J16 connector
J12 Pins 5, 9 – 15, 17 – 20	Negative pulses at 16ms rate	J16 connector
J12 Pin 6	768kHz square wave	J16 connector

Table 6-18. J16 (Microprocessor/Synthesizer Board) Signals (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
J12 Pins 7 and 8	High	J16 connector
J16 pin 16	Small burst of narrow pulses at Power On with scope Trig Source set to Normal, Trig Slope set to Negative and Intensity increased.	Address Decoder (paragraph 6.3.11)

6.3.19 RS-232-C

Related information in this manual.
Schematic: 0103-00-1677 Sheet 1.
Circuit Description: Paragraph 4.4.2.

All components referenced in this paragraph are located on the option board unless otherwise specified.

Refer to table 6-19 to fault isolate the RS-232-C and associated circuitry.

Table 6-19. RS-232-C Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
Front Panel (Rear panel Interface disconnected)	Proper local control	If abnormal operation with J16 disconnected, U3 (microprocessor/synthesizer board paragraph 6.3.1) or associated circuitry.
		If normal operation with J16 (microprocessor/ synthesizer board) disconnected, check for a "stuck" bit at J16.
Display (Rear panel Interface disconnected)	"WAVETEK MODEL 23 OPT 002 RS-232-C" momentarily after cycling Power Off, then On.	Y1 or incorrect signal on a J16 line. See table 6-18.
Display	If "WAVETEK MODEL 23 OPT 002 RS-232-C" displayed at turn On, use the STATUS and ◄ buttons to display "hand CTS/DTR".	U1.
U1 pins 3 and 4	153.6kHz TTL square with factory setting of 9600 baud at SW-1 (SW1-4 open, 3 closed, 2 closed and 1 closed).	SW-1, U2 or U1
U1 pins 3 and 4	16X selected baud rate of rate of sending device if different from 9600 baud (see paragraph 2.2.7 of this manual).	SW-1, U2 or U1

Table 6-19. RS-232-C Fault Isolation (Continued)

(Rear panel interface disconnected for the following readings)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U1 pin 2	High	If any reading incorrect, U1, U3 or U4 could be bad.
U1 pin 5	Low	
U1 pin 6	High	
U1 pin 23	Low with SW1-5 open and high with SW1-5 closed.*	
U1 pin 24	High	
U3 pins 3 and 6	~ +15V	
U3 pin 8	~ −15V	
U3 pin 11	~ +15V	
U4 pin 1	~ 0V	
U4 pin 4	~ 0V	
U4 pin 8	High	
U4 pin 10	Low	

* Return SW1-5 to open.

Verify correct:

Baud rate;
DCE/DTE configuration;
CTS/DTR or XON/XOFF.

Verify the option board is configured properly, then connect the RS-232-C cable to the rear panel. If problem remains, U1 or W15 connections could be bad.

6.3.20 VCG

Related information in this manual.
Schematic: 0103-00-1455 Sheet 1.
Circuit Description: Paragraph 4.6.1.
Calibration Procedure: Table 5-1, Steps 5, 16, and 21.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then set the controls as indicated in table 6-20, and take the measurements.

Table 6-20. VCG

Frequency	J7-10 (J7 Pin 1 is Nearest to R184)	U23-7
10.0kHz	+1.0V	−0.9V
99.9kHz	+10.0V	−9.0V

Related digital control lines.
SYNTH: TTL Low = VCG In connected;
TTL High = VCG In disconnected.

6.3.21 Current Source and Sink

Related information in this manual.
Schematic: 0103-00-1455 Sheet 1.
Circuit Description: Paragraph 4.6.1.
Calibration Procedure: Table 5-1, Steps 17, 18, and 19.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then set the controls as indicated in tables 6-21 and 6-22 and take the measurements.

Table 6-21. Current Source

Frequency	U23-7	J15-1	U23-8	U25-10
10.0kHz	−0.9V	0.0V	~ +5.7V	~ +14.6V
99.9kHz	−9.0V	0.0V	~ +2.0V	~ +10.5V

Table 6-22. Current Sink

Frequency	R23-3	J15-1	U23-1	U25-4
10.0kHz	−0.4V	+0.00V	~ −5.7V	~ −14.6V
99.9kHz	−4.0V	+0.00V	~ −2.0V	~ −10.5V

6.3.22 Trigger Control Current Sink

Related information in this manual.
Schematic: 0103-00-1455 Sheet 1.
Circuit Description: Paragraph 4.6.1.
Calibration Procedure: Table 5-1, Step 30.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then set the controls as indicated in table 6-23 and take the measurements.

Table 6-23. Current Sink and Trigger Control

Frequency	U25-1/Q21 Base	U25-7/Q21 Emitter
10.0kHz	∿ – 14.0V	– 14.6V
99.9kHz	∿ – 10.3V	∿ – 11.0V

Press "Reset", then set the controls as indicated in table 6-24 and take the measurements.

Press "Reset", change the frequency to 99.9kHz, then set the controls as indicated in table 6-25 and take the measurements.

6.3.23 Current Switch

Related information in this manual.
Schematic: 0103-00-1455 Sheet 2.
Circuit Description: Paragraph 4.6.2.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then take the measurements as shown in figure 6-1.

6.3.24 Frequency Range Switches

Related information in this manual.
Schematic: 0103-00-1455 Sheet 1.
Circuit Description: Paragraph 4.6.3.
Calibration Procedure: Table 5-1, Step 21.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Table 6-26 lists the logic levels for the nine frequency ranges; a TTL low ("0") enables the range capacitor, and a TTL high ("1") disables the range capacitor. To check the logic levels, press "Reset" and set the instrument to the desired frequency.

Table 6-24. Trigger Control

Mode	CR28 Anode (RUN)	CR26 Anode	CR26 Cathode	U22-9 (TRN)
Cont	TTL High	+ 2.3V	+ 1.7V	± 1V Triangle
Trig	TTL Low	– 1.1V	– 0.7V	0.0V

Table 6-25. Trigger Control

Mode	CR28 Anode (RUN)	CR26 Anode	CR26 Cathode	U22-9 (TRN)
Cont	TTL High	+ 2.0V	+ 1.3V	± 1V Triangle
Trig	TTL Low	– 1.1V	– 0.75V	0.0V

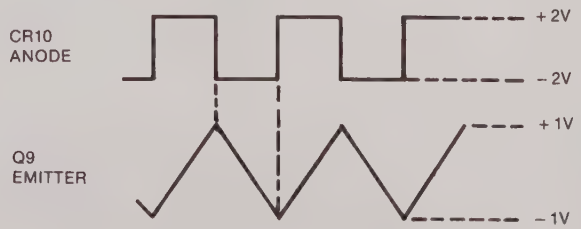


Figure 6-1. Current Switch Waveforms

Table 6-26. Frequency Control

Min Freq (Hz)	Max Freq (Hz)	U1-5 (LF)		J7-1* (FR7)	J7-3* (OVRNG)	J7-4* (FR4)	J7-5* (FR6)	J7-6* (FR5)	J7-13* (LF)		J7-20* (100)
10.00MHz	12.000MHz	0		0	0	1	1	1	1		1
1.000MHz	9.999MHz	0		0	1	1	1	1	1		1
100.0kHz	999.9kHz	0		1	1	1	0	1	1		1
10.00kHz	99.99kHz	0		1	1	1	1	0	1		1
1.000kHz	9.999kHz	0		1	1	0	1	1	1		1
		DC Func	Other Func's						DC/Sq Func's	Other Func's	
100.0Hz	999.9Hz	0	1	1	1	1	0	1	1	0	1
10.00Hz	99.99Hz	0	1	1	1	1	1	0	1	0	1
1.000Hz	9.999Hz	0	1	1	1	1	0	1	1	0	0
100.0mHz	999.9mHz	0	1	1	1	1	1	0	1	0	0
10.00mHz	99.99mHz	0	1	1	1	0	1	1	1	0	0

*J7 pin 1 is nearest to R184.

Table 6-27 gives measurement values for a single typical range switch (FR6); these levels are typical of all three switches.

Table 6-27. Frequency Range (FR6 shown, typical)

Test Point	Low (Enabled)	High (Disabled)
Base Q1	+ 4.2 Vdc	+ 5.1 Vdc
Emitter Q1	+ 4.3 Vdc	+ 4.3 Vdc
Collector Q1	+ 5.0 Vdc	– 15 Vdc
CR5 anode	+ 1.5 Vdc	– 15 Vdc
R4 (right side)	– 7.5 Vdc	– 7.5 Vdc

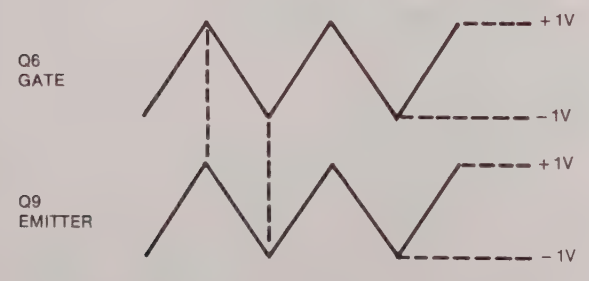


Figure 6-2. Triangle Buffer (Cont Mode)

6.3.25 Triangle Buffer

Related information in this manual.
Schematic: 0103-00-1455 Sheet 2.
Circuit Description: Paragraph 4.6.4.
Calibration Procedure: Table 5-1; Step 30.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then take the measurements as shown in figure 6-2.

Change Mode to Trigger, then take the measurements as shown in table 6-28.

Table 6-28. Triangle Buffer (Trigger Mode)

Test Point	Desired Result
Q6 Gate	0.0V
Q6 Source	+ 0.5V*
Q9 Base	– 0.65V*
Q9 Emitter	0.0V*

*Varies with R26 setting.

6.3.26 Comparator, Switch and Square Buffers

Related information in this manual.
Schematic: 0103-00-1455 Sheet 2.
Circuit Description: Paragraphs 4.6.5, 4.6.6, and 4.6.8.

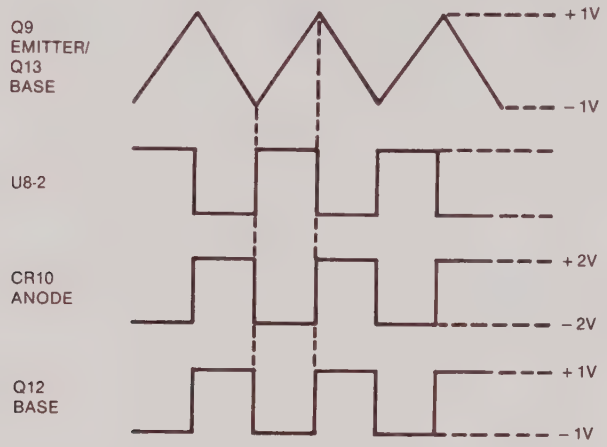


Figure 6-3. Comparator, Switch and Square Buffer

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then take the measurements as shown in figure 6-3.

6.3.27 High Frequency Compensation

Related information in this manual.
Schematic: 0103-00-1455 Sheet 1.
Circuit Description: Paragraph 4.6.7.
Calibration Procedure: Table 5-1, Step 21.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", then take the measurements as shown in table 6-29.

Table 6-29. Low Frequency Check (<1MHz)

Test Point	Desired Result
U23-12	0.0Vdc
U23-13	0.0Vdc
U23-14	+0.7Vdc
Q20 Collector	+6.9Vdc
Q18 Base	–6.9Vdc
Q19 Emitter	+7.5Vdc
Q18 Emitter	–7.5Vdc

Change frequency to 12MHz, then take the measurements as shown in table 6-30.

Table 6-30. High Frequency Compensation (1MHz to 12MHz)

Test Point	Desired Result
U23-12	∿ –9.0Vdc
U23-14	∿ –8.5Vdc
Q20 Collector	∿ +11.5Vdc
Q18 Base	∿ –11.5Vdc
Q19 Emitter	∿ +12.0Vdc
Q18 Emitter	∿ –12.0Vdc

*Varies with R66 setting.

Related digital control logic.
Below 1MHz, FR7 remains high.
At 1MHz and above, FR7 goes low.

6.3.28 Trigger Logic

Related information in this manual.
Schematic: 0103-00-1455 Sheet 3.
Circuit Description: Paragraph 4.6.9.

All components referenced in this paragraph are located on the waveform generator board uniess otherwise specified.

Table 6-31 lists the control lines related to the trigger logic circuit.

Table 6-31. Trigger Logic Truth Table

	U18-1 (MC0)	U9-4 (MC1)	U3-4 (KILL)	U1-5 (LF)	U3-6 (RUN)
Cont	TTL Low	TTL High	—	—	TTL High
Trig	TTL High	TTL Low	—	—	TTL Low unless triggered
Gate	TTL High	TTL High	—	—	TTL Low unless triggered
					TTL High from trigger input to end of last cycle
Synth	TTL Low	TTL High	—	—	TTL High
DC Function	—	—	TTL Low	—	TTL Low
All but DC Function	—	—	TTL High	—	TTL High unless in Trig or Gate (see above)
10mHz to 999.9Hz	—	—	—	TTL high	—
999.9Hz to 32MHz	—	—	—	TTL Low	—

6.3.29 Frequency Synthesizer

Related information in this manual.
Schematic: 0103-00-1454 Sheet 2.
Circuit Description: Paragraph 4.7.

All components referenced in this paragraph are located on the microprocessor/synthesizer board unless otherwise specified.

Press "Reset", then take the measurements as shown in table 6-32.

Table 6-32. Frequency Synthesizer Loop Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
Func Out	Proper operation in continuous mode.	Paragraphs 6.3.12 and 6.3.20 thru 6.3.27
For remaining checks in this table, set Mode to Clock.		
ECL or TTL Out	If signal is normal, go to paragraph 6.3.30.	Continue with this table.

For the remaining tests in this table, disconnect J6 and, if installed, remove option 001 or 002 board on microprocessor/synthesizer board.

CAUTION

Prevent J6 pins from shorting to any point.

Table 6-32. Frequency Synthesizer Loop Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U31 pin 6	TTL square at programmed frequency (1kHz to 12MHz). If good, problem caused by coax cable, U27 or input lines SA, SB (paragraph 6.3.8) or FGSYNC.	Continue with this table.
U22 pins 10 and 11	Low duty cycle TTL positive pulse activity as knob rotated. (Set scope intensity high)	U22 or U3
U22 pin 12	Low duty cycle TTL positive pulse activity as knob rotated. (Set scope intensity high)	Go to paragraph 6.3.11.
U26 pin 1	~ +5.0Vdc	SYNTH input line or Q11 and associated circuitry.
U23 pin 7	~ +3.5Vdc to ~ −8.5Vdc as VCO frequency at U26 pin 11 varies from 32MHz to 64MHz. If good, go to table 6-33.	Continue with this table.
Jumper U23 pin 5 to ground for the following tests.		
U23 pin 7	0Vdc	U23
U26 pin 11	TTL compatible, ramplike waveform at ~ 40-45MHz.	VCO circuit of Q5-Q10
U26 pins 8 & 9	TTL square at 1/2 the frequency of pin 11	If pins 1 and 13 are low, Q11 or SYNTH signal (paragraph 6.3.8)
		If pins 1 and 13 are high, U26.
U25 pin 2	~ 10MHz	U26, U25 or U24
U25 pin 14	~ 5MHz	U25 or U24
U25 pin 13	~ 2.5MHz	U25 or U24
U25 pin 12	~ 1.25MHz	U25 or U24

Table 6-32. Frequency Synthesizer Loop Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U22 pin 9	~1.25MHz with programmed frequency of 1MHz to 1.999MHz, ~2.5MHz from 2MHz to 3.999MHz, ~5MHz from 4MHz to 7.999MHz and ~10MHz from 8MHz to 32MHz.	U22, U24
U22 pin 6	0V from 1MHz to some switch point lower than 1.999MHz (usually near 1.3MHz). +5V from switching point to 1.999MHz	U22 or U23
U23A pin 1	Near +15Vdc when frequency below switch point in prior step. Near −15Vdc when frequency above switch point in prior step.	U23
Remove jumper shorting U23 pin 5 to ground.		

Press "Reset", set frequency to 10MHz and mode to clock, then take the measurements as shown in table 6-33.

Reconnect J6 and replace option board, then go to paragraph 6.3.42 and verify sync outputs.

6.3.30 1:1 Lock Loop

Do this paragraph only if paragraph 6.3.29 has already been attempted.

Related information in this manual.
Schematic: 0103-00-1455 Sheet 6.
Circuit Description: Paragraph 4.8.
Calibration Procedure: Table 5-1, Step 5.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set mode to synthesized, then take the measurements as shown in table 6-34.

Table 6-33. Frequency Synthesizer Divider Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U30 pin 9	10MHz	U24, U28 or U29
U30 pin 12	1MHz	U24, U28 or U29
U30 pin 6	100kHz	U24, U28 or U29
U30 pin 2	10kHz	U24, U28 or U29

Table 6-33. Frequency Synthesizer Divider Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U30 pin 8	TTL Low	Front panel (paragraph 6.3.3)
U30 pins 3, 5 and 11	TTL High	Front panel (paragraph 6.3.3)
U31 pin 13	10MHz	U30
U31 pins 9, 10 and 12	TTL Low	U30
U31 pins 2 through 6 and 11	10MHz	U31
U31 pin 1	TTL Low	U31
U27 pin 12	10MHz	Coax Cable
U27 pin 6	TTL Square wave across entire programmed frequency	U27, SA, SB or coax
U15 pin 5 (Waveform generator board)	TTL Square wave across entire programmed frequency	U27, SA, SB or coax

Table 6-34. 1:1 Lock Loop Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U29 pin 1	TTL square at programmed frequency, 1kHz to 12MHz.	Coax cable.
U29 pin 3	TTL square at function gen-generator frequency, 1kHz to 12MHz.	Coax cable or square selector (paragraph 6.3.36).
U29 pins 1 and 3	Frequencies equal	1:1 loop normal. Go to figure 6-1 for another starting point.
J15 pin 4	Not saturated at ±6Vdc at any frequency.	1:1 loop normal. Go to figure 6-1 for another starting point.
U26 pins 6 and 7	Voltages identical	U26 or associated circuitry. Verify SYNTH low (paragraph 6.3.8).

Table 6-34. 1:1 Lock Loop Fault Isolation (Continued)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U29 pins 8 and 9	+1.4Vdc	U28 or U29 circuitry.
U29 pins 2 and 13	If HFSQ frequency lower than FSYNTH: pin 13 low, pin 2 high. If HFSQ frequency higher than FSYNTH: pin 13 high, pin 2 low.	U29
Q42 base	~+6.2Vdc	U28, Q42 or Q43 circuitry
Q43 base	~−6.2Vdc	U28, Q42 or Q43 circuitry
Across R190	~8.1Vdc	U28, Q42 or Q43 circuitry
Across R186	~8.1Vdc	U28, Q42 or Q43 circuitry
Across R185	~8.1Vdc	U28, Q42 or Q43 circuitry
Right end of R187	~−6.9Vdc	U28, Q42 or Q43 circuitry
Q42 collector	~ +6.5V if U29 pin 13 low. ~ −6.5V if U29 pin 2 low.	U28, Q42 or Q43 circuitry
Q45 Emitter (VLOOP)	Q42 collector voltage +~1V ±1V.	Q44 or Q45 circuitry

Check the setting of R184 and the circuitry around U32 range switches and loop filter components connected between the collector of Q42 and the gate of Q44.

Related information in this manual.
Schematic: 0103-00-1455 Sheet 3.
Circuit Description: Paragraph 4.9.
Calibration Procedure: Table 5-1, Step 23.

6.3.31. Waveform Synthesizer

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set frequency to 100Hz, then take the measurements as shown in tables 6-35 and 6-36.

Table 6-35. Function Select Control Line Fault Isolation

Function	Normal Reading At U19 Pin 1 (FSO)	Normal Reading At Feed-Through Between Ends Of U10 And U11 (FS1)
DC	TTL Low	TTL Low
Sine	TTL Low	TTL Low
Square	TTL Low	TTL Low
Triangle	TTL Low	TTL High
Rmp Up	TTL High	TTL Low
Rmp Dn	TTL High	TTL High

Table 6-36. Waveform Synthesizer Fault Isolation

Test Point	Normal Reading	Possible Cause of Wrong Reading
U30-8 (LF)	Low.	Analog Interface (paragraph 6.3.8), J6, J7, function selector (paragraph 6.3.34).
U6 pin 2 (MFSQ)	100kHz Clock pulses	Square selector (paragraph 6.3.36).
U4 pin 3, U7 pins 7, through 1, U7 pin 23	Data lines change	U4, U6, U13 or associated circuitry
U13 pin 1	Test point switching coincident with positive and negative triangle peaks at Func Out on dual trace scope. Sink to test point.	U3 or associated circuitry
U14 pins 3, 4, 7, 8, 13, 14, 17 and 18	Data lines change	U7 or associated circuitry
U21 pins 5 through 12	Data lines change	U14 or associated circuitry
U21 pin 4 (DAC output)	Correct waveform	U21 or associated circuitry

6.3.32 Sine Converter

Related information in this manual.
Schematic: 0103-00-1455 Sheet 4.
Circuit Description: Paragraph 4.11.1.
Calibration Procedure: Table 5-1, Steps 20 and 26.

Note

Time symmetry and dc offset of triangle affects the sine distortion; refer to the calibration procedure, steps 18, 19, 20, 26 and 30.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset" then take the measurements as shown in figure 6-4.

Below 1kHz, the sine converter has no affect on the sine wave because it's created by the waveform synthesizer.

6.3.33 Function Selector

Related information in this manual.
Schematic: 0103-00-1455 Sheet 4.
Circuit Description: Paragraph 4.11.2.
Calibration Procedure: Table 5-1, Steps 27 and 28.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

The function selector, which consists of three switches, routes the various functions to the preamplifier. Only one switch will be closed at a time.

Table 6-37 describes all function control lines. A TTL low ("0") originating from the microprocessor section enables the respective function selector switch or logic gate. A TTL high ("1") disables the function selector switch or logic gate.

6.3.34 Preamplifier

Related information in this manual.
Schematic: 0103-00-1455 Sheet 4.
Circuit Description: Paragraph 4.11.3.
Calibration Procedure: Table 5-1, steps 8 and 14.

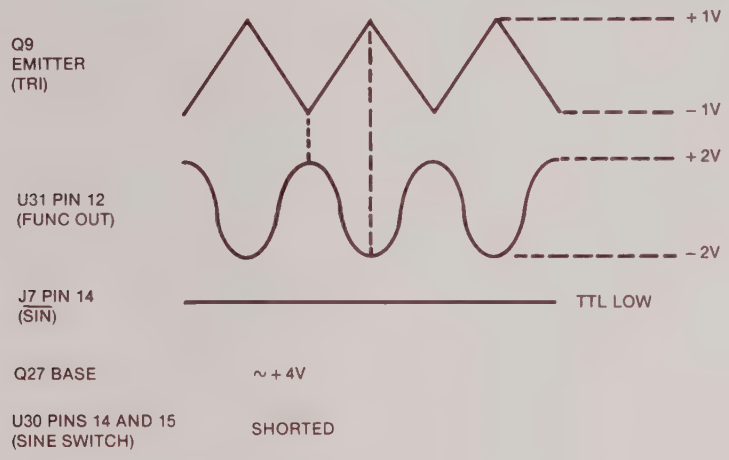


Figure 6-4. Sine Converter

Table 6-37. Function Control Lines

Freq	Function	U1-5 (LF)	J7-13* (LF)	@ (SIN)	c (SQR)	# (TRI)	U3-4 (KILL)	U19-1 (FSO)	** (FS1)
>1kHz	DC	0	1	1	1	1	0	0	0
	Sine	0	1	0	1	1	1	0	0
	Square	0	1	1	0	1	1	0	0
	Triangle	0	1	1	1	0	1	0	1
	Ramp Up	—	—	—	—	—	—	—	—
	Ramp Dn	—	—	—	—	—	—	—	—
≤1kHz	DC	0	1	1	1	1	0	0	0
	Sine	1	0	1	1	1	1	0	0
	Square	1	1	1	0	1	1	0	0
	Triangle	1	0	1	1	1	1	0	1
	Ramp Up	1	0	1	1	1	1	1	0
	Ramp Dn	1	0	1	1	1	1	1	1

* J7 pin 1 is nearest to R184.
@ Right end of R164 (viewed from front of instrument)
c Right end of R144 (viewed from front of instrument)
Right end of R167 (viewed from front of instrument)
** Feed-through between ends of U10 and U11.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

DC Problems

Press "Reset", set function to DC, then take the measurements as shown in table 6-38.

Table 6-38. Preamplifier Voltage Check in DC Function

Test Point	Desired Result
Right end of R150	~ −0.7Vdc
J15-6	~ 0Vdc
Right end of R141	~ 0Vdc
Right end of R134	~ 0Vdc
Q31 base	+6.0Vdc
Q32 base	−6.0Vdc
Across R137	~ 0.5Vdc
CR33 anode	+10.0Vdc
Q29 emitter	+10.0Vdc

Waveform Problems

Press "Reset", set amplitude to maximum, then take the measurements as shown in table 6-39.

Table 6-39. Preamplifier Voltage Checks in Sine Function

Test Point	Desired Result
Right end of R150	~ 0.7Vdc
J15-6	±0.5V sine wave
Right end of R141	±0.5V sine wave
Right end of R134	~ 0Vdc
Q31 base	+6.0Vdc
Q32 base	−6.0Vdc
Across R137	~ 0.5Vdc
CR33 anode	+10.0Vdc
Q29 emitter	+10.0Vdc

6.3.35 Square Selector

Related information in this manual.
Schematic: 0103-00-1455 Sheet 3.
Circuit Description: Paragraph 4.11.4.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set frequency as specified, then take the measurements as shown in table 6-40.

Table 6-40. Square Selector

Programmed Frequency	U1-5 (LF Control Line)	Square Source	TTL Out	Right End Of R124 (TTLSQR)	U8-3 (HFSQ)	U15 pin 8 (FGSYNC)
≥1.00 kHz	Low	SWSQR (Function Generator)	TTL square wave in phase with U8-2 (SWSQR)	TTL square wave at Func Out frequency when in square function	TTL square wave at function generator when in synthesizer mode	TTL square wave at Func Out frequency
<1.00 kHz	High	U4-6 (Waveform Synthesizer)	TTL square wave in phase with U4-6	TTL square wave at Func Out frequency when in square function	TTL square wave at function generator frequency when in synthesizer mode	TTL square wave at Func Out frequency

6.3.36 Square Shaper

Related information in this manual.
Schematic: 0103-00-1455 Sheet 4.
Circuit Description: Paragraph 4.11.5.
Calibration Procedure: Table 5-1, Step 29.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set function to square, then take the measurements as shown in figure 6-5.

Verify U1 pin 3 (SQR) low only when square function selected.

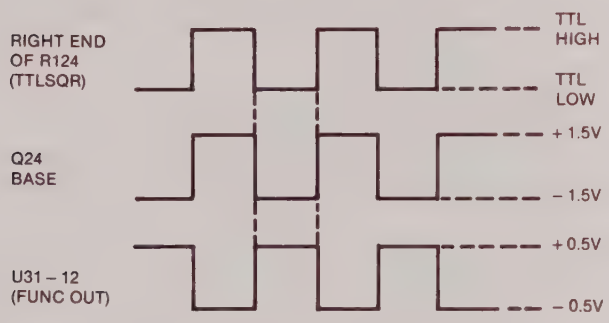


Figure 6-5. Square Shaper

6.3.37 XY Multiplier

Related information in this manual.
Schematic: 0103-00-1455 Sheet 5.
Circuit Description: Paragraph 4.11.6.
Calibration Procedure: Table 5-1, Steps 7, 12 and 22.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set amplitude to maximum, function to DC, then take the measurements as shown in table 6-41.

Table 6-41. Preamplifier Voltage Checks In Sine Function

Test Point	Desired Result
U31-12	0V
U31-2 and 14	+7.5V
U31-4	+1V
U31-8	+1.2V

6.3.38 Output Amplifier

Related information in this manual.
Schematic: 0103-00-1455 Sheet 5.
Circuit Description: Paragraph 4.11.7.
Calibration Procedure: Table 5-1, steps 9, 10, 13, 24, 25 and 31.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set function to DC, then take the measurements as shown in table 6-42.

Table 6-42. Output Amplifier

Test Point	Desired Results
Left end of R240	~0Vdc
U31 pin 2	+7.8Vdc
U31 pin 14	+7.8Vdc
U33 pin 4	+0.3Vdc
U33 pin 5	+0.3Vdc
U33 pin 6	–13Vdc
U33 pin 10	~0Vdc
U33 pin 11	+13Vdc

6.3.39 Output Attenuator

Related information in this manual.
Schematic: 0103-00-1455 Sheet 6.
Circuit Description: Paragraph 4.11.8.

CAUTION

Terminate the Func Out with 50Ω load.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset" then take the measurements as shown in table 6-43.

Table 6-43. Attenuator

Test Point	Amplitude Setting	Desired Result
A_0*	5Vp-p	TTL Low
A_1**	5Vp-p	TTL Low
A_0*	500mVp-p	TTL Low
A_1**	500mVp-p	TTL High
A_0*	50mVp-p	TTL High
A_1**	50mVp-p	TTL High

* Right end of C174 (viewed from front of instrument)
** Right end of C173 (viewed from front of instrument)

Table 6-44. TTL Driver

Frequency Setting	SA*	SB**	Sync Source
< 1kHz	TTL Low	TTL Low	Waveform synthesizer (FGSYNC)
1kHz to 12MHz	TTL High	TTL High	FSYNTH
12MHz to 16MHz	TTL Low	TTL High	U27 pin 14 (microprocessor/synthesizer board)
16MHz to 32MHz	TTL High	TTL Low	U27 pin 13 (microprocessor/synthesizer board)

* U14 pin 19 on microprocessor/synthesizer board. ** U14 pin 16 on microprocessor/synthesizer board.

6.3.40 Function Output Protection

Related information in this manual.
Schematic: 0103-00-1455 Sheet 6.
Circuit Description: Paragraph 4.11.8.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset" then check for 5Vp-p (10Vp-p unloaded) sine wave at the Function Out BNC.

WARNING

POWER MUST BE TURNED OFF BEFORE CHECKING FUSE AND DIODES.

If no signal is present, check fuse (F3) and damaged diodes (CR53, CR54, CR55, CR56).

6.3.41 TTL Driver

Related information in this manual.
Schematic: 0103-00-1455 Sheet 6.
Circuit Description: Paragraph 4.12.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Press "Reset", set mode to clock, then take the measurements shown in table 6-44.

6.3.42 ECL Driver

Related information in this manual.
Schematic: 0103-00-1455 Sheet 6.
Circuit Description: Paragraph 4.12.

Press "Reset".

Refer to paragraph 6.3.41 if TTL Out signal not normal.

All components referenced in this paragraph are located on the waveform generator board unless otherwise specified.

Take the measurements as shown in table 6-45.

Table 6-45. ECL Driver

Test Point	Desired Result
Q38 Base	TTL level square wave
Q39 Base	+6.5Vdc
Q40 Base	Square wave at levels of +0.2V and −1.3V.
Q41 Base	+1.4Vdc

6.3.43 Power Supply

Related information in this manual.
Schematic: 0103-00-1113 Sheet 1.
Circuit Description: Paragraphs 4.13, 4.13.1 and 4.13.2.
Calibration Procedure: Table 5-1, steps 1 through 3.

To replace fuse, refer to paragraph 2.2.3.

All components referenced in this paragraph are located on the power supply board unless otherwise specified.

Check voltages given in table 6-46 to determine a faulty power supply.

Table 6-46. Power Supply

Supply	Voltage Tolerance	Test Point	Maximum Input Ripple	Test Point	Maximum Output Ripple	Test Point
+15V	±350mV	VR1-14	3Vac	VR1-3	0.02Vac	VR1-14
−15V	±350mV	VR1-7	3Vac	VR1-4	0.02Vac	VR1-7
+5V	±250mV	VR2 top lead	3Vac	VR2 bottom lead	0.02Vac	VR2 top lead

If an input measures bad, remove power and connector J3, then check for:

(a) Blown fuse.

(b) Shorted or open diodes (CR1, CR2).

(c) Shorted or open capacitors (C2, C3, C4, C5, C10, C11) at the input of the pass devices.

(d) Short between the pass devices' metal mounting tab and chassis ground.

(e) Bad transformer.

If all inputs measure good, remove power and connectors J4 and J5, then check for:

(a) Shorted capacitors at the regulator's output.

(b) Short between pass devices' metal mounting tab and chassis ground.

(c) Excessive loading by board circuits; to verify, disconnect by removing either J4 or J5.

(d) Check +15V and −15V pass devices for normal transistor operation.

(e) If all of the above conditions appear normal, replace the voltage regulator; VR1 for +5V and VR2 for +15V and −15V.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than 1Vdc is measured across its base-emitter junction in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage across the base-emitter junction.
3. If the collector and emitter voltages are the same, but the base-emitter voltage is less than 500 mV forward voltage or reversed bias, the transistor is defective.
4. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base-emitter junction should be off (no collector current); otherwise one of the transistors is defective.

6.4.2 Diode

1. A diode (except a zener) is defective if there is greater than 1Vdc (typically 0.7Vdc) forward voltage across it.

6.4.3 Operational Amplifier

1. Generally the "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operation amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No measurable gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective. Gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485 and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors can often be located by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

The number etched into a PC board is the board part number. The assembly (PC board and components on the board) part number is stamped on the board.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0360
Instrument Top Assembly/Parts List	1000-00-0360
Chassis Assembly/Parts List	1101-00-1700
Front Panel Schematic	0103-00-1701
Front Panel Assembly/Parts List	1201-00-1701
Keyboard Assembly/Parts List	1208-00-1376
Rear Panel Assembly	1101-00-1703
Rear Panel Parts List	1101-00-1703
Microprocessor/Synthesizer Board Schematic	0103-00-1454
Microprocessor/Synthesizer Board Assembly	1100-00-1454
Microprocessor/Synthesizer Board Parts List	1100-00-1454
Waveform Generator Board Schematic	0103-00-1455
Waveform Generator Board Assembly	1100-00-1455
Waveform Generator Board Parts List	1100-00-1455
Power Supply Schematic	0103-00-1113
Power Supply Assembly/Parts List	1208-00-1118
AC Primary Assembly/Parts List	1208-00-1119
GPIB Option Assembly/Parts List	1000-00-0426
GPIB Option Schematic	0103-00-1678
GPIB Option P.C.A. Assembly/Parts List	1100-00-1678
RS-232-C Option Assembly/Parts List	1000-00-0427
RS-232-C Option Schematic	0103-00-1677
RS-232-C Option P.C.A. Assembly/Parts List	1100-00-1677

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REV	ECN	BY	DATE	APP
A	4921	DT	10/8/85	R.R.T.
B	6080	DT	1/10/86	R.R.T.

A1
ASSY,
FRONT PANEL
1201-00-1701

AIA4 PCA, DISPLAY
1208-00-1874

AIA3 PCA, KEYBOARD
1208-00-1376

W17
(OPTION 001 ONLY)

P30 J30 — OPTION 001 — J17 W8 W15 E40
COM: NC, NC, NC, NC, NC, NC, NC
REN, DIO8, DIO7, DIO6, DIO5, NC, GROUND, ATN, SRQ, IRC, NDAC, NRFD, DAV, EOI, DIO4, DIO3, DIO2, DIO1
PCA, GPIB OPTION
1100-00-1678

J29 W15
ASSY,
REAR PANEL
1206-00-1906

P30 J30C — OPTION 002 — J17 W8 W15
TDX, RXD, —, CTS, DSR, SIG GND, RLSD, —, —, —, —, —, —, —, —, —, —, DTR, —, —, —, —, —
DCE CONNECTOR
PCA, RS232 OPTION
1100-00-1677

P30 J30T W15
TDX, RXD, RTS, CTS, DSR, SIG GND, RLSD, —, —, —, —, —, —, —, —, —, —, DTR, —, —, —, —, —
DTE CONNECTOR

P16 J16 W8
GND, +5V, +15V, -15V, R/W, E, IRQ, MR, AD4, AD5, AD6, AD7, ADRØ, ADR1, ADR2, COMM, ADØ, AD1, AD2, AD3

A3
PCA, μPROC/SYNTHESIZER
1100-00-1454

J11 W5 P10 J10
GND, +5V, DD, ADRØ, R/W, DE, ADØ, AD1, AD2, AD3, AD4, AD5, AD6, AD7

J13 W6 P12 J12
IN1-Ø, IN1-2, IN1-4, IN1-6, INØ-6, INØ-5, IN1-5, INØ-7, GND, DDH, DD, DDL, INØ-4, INØ-3, INØ-2, INØ-1, INØ-Ø

J6 P6
FR7, SYNTH, OVRNG, FR4, FR6, FR5, GND, VNULL, VAMP, VFREQ, VOFST, GND, LF, SIN, TRI, AØ, A1, KILL, MCØ, ÷100

J9 J8 J14

W1 W2 W7 W9

J7
E28 E29 E30 E31 E32 E33

P4 J4
1A TRIG EN
2A FSØ
3A TRIG SLOPE
4A MC1
5A -15V
6A +5V
7A +5V
8A +15V
9A HAV
10A FS1
1B GND
2B GND
3B —
4B —
5B GND
6B GND
7B SQR
8B LF
9B GND
10B GND

P5 J5
1A TRIG EN
2A FSØ
3A TRIG SLOPE
4A MC1
5A -15V
6A +5V
7A SQR
8A +15V
9A HAV
10A FS1
1B GND
2B GND
3B —
4B —
5B GND
6B GND
7B GND
8B LF
9B GND
10B GND

J15 — TEST CONNECTOR
VCG TEST, +5V, GND, LOOP TEST, VCV TEST, FUNC TEST, -15V, -15V, —, RUN TEST, —, —, TRI TEST, +15V

A4
PCA, WAVEFORM GEN
1100-00-1455

J18 VCG IN — J19 TRIG IN — J20 AM IN — J21 TTL SYNC (50Ω) — J22 ECL SYNC 50Ω — J23 FUNC OUT

J1 AC POWER E1 E2 E3 W3 W4

A2A2
PCA, AC PRIMARY
1208-00-1119

✱P2, P32 SHOWN IN 115, HI POSITION

J32 P32 — J2 P2
BLK, ORN, GRY, VIO, YEL, WHT/BLK, WHT/GRY, WHT

T1
1204-00-1860

RED, RED, WHT/RED, BLU, BLU
P3 J3

A2
ASSY, REAR PANEL
POWER SUPPLY
1101-00-1703

A2A3
PCA, POWER SUPPLY
1208-00-1118

MODEL 23
STANDARD -(1000-00-0360)
GPIB, OPTION-001 (1000-00-0426)
RS-232, OPTION-002 (1000-00-)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN A.TALMADGE 1/10/85
PROJENGR 1/15/85
RELEASE APPROV 1/24/85
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA
TITLE: SCHEMATIC, INSTRUMENT
MODEL NO 23
DWG NO. 0004-00-0360
REV B
CODE IDENT 23338
SHEET 1 OF 1

0004-00-0360 B

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REV	ECN	BY	DATE	APP
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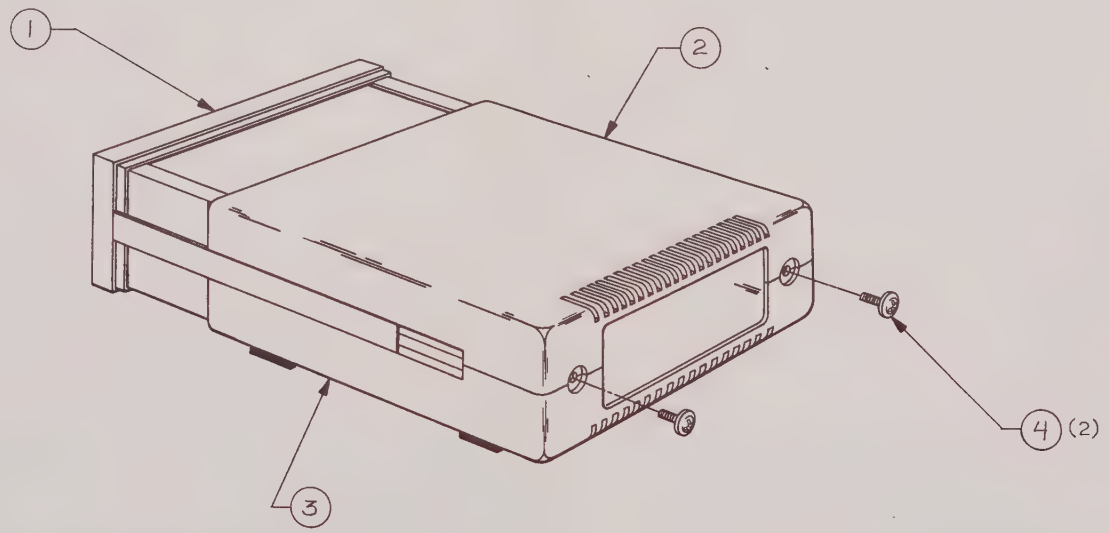

A1

MODEL 23
12 MHz SYNTHESIZED FUNCTION GENERATOR
1000-00-0360

- A1A1 ASSY, CHASSIS 1101-00-1700
  - A1A1A1 ASSY, FRONT PANEL 1201-00-1701
    - A1A1A1A1 ASSY, ENCODER KNOB 1201-00-1731
    - A1A1A1A2 FRONT HOUSING (SCREENED) 1201-00-8659
      - A1A1A1A2A1 SUBASSY, FRONT HOUSING 1201-00-1702
    - A1A1A1A3 PCA, KEYBOARD 1208-00-1376
    - A1A1A1A4 PCA, DISPLAY 1208-00-1874
  - A1A1A2 ASSY, REAR PANEL/ POWER SUPPLY 1101-00-1703
    - A1A1A2A1 SUBASSY, REAR PANEL 1206-00-1906
    - A1A1A2A2 PCA, AC PRIMARY 1208-00-1119
    - A1A1A2A3 PCA POWER SUPPLY 1208-00-1118
      - A1A1A2A3A1 ASSY, HEATSINK BRKT 1201-00-1707
    - A1A1A2A4 ASSY, FUSE COVER 1201-00-1585
    - A1A1A2A5 TRANSFORMER 1204-00-1860
  - A1A1A3 PCA, UPROC/SYNTHESIZER 1100-00-1454
  - A1A1A4 PCA, WAVEFORM GEN 1100-00-1455
  - A1A1A5 ASSY, CABLE KIT 1207-00-1705
- A1A2 ASSY, TOP COVER 1201-00-1114
- A1A3 ASSY, BOTTOM COVER 1206-00-1301
  - A1A3A1 ASSY, BOTTOM COVER 1201-00-1136

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, OUTLINE-23	0002-00-0360	WVTK	0002-00-0360	1
NONE	SCHEMATIC, INSTRUMENT	0004-00-0360	WVTK	0004-00-0360	1
1	ASSY, CHASSIS-23	23-1700	WVTK	1101-00-1700	1
2	ASSY, TOP COVER	21-1114	WVTK	1201-00-1114	1
3	ASSY, BOTTOM COVER	1206-00-1301	WVTK	1206-00-1301	1
NONE	INSTRUCTION MANUAL	MANUAL-23	WVTK	1300-00-0360	1
4	SCREW, TRUSS HD, CAD I, PHLPS, 10-32X1/2	10-32X1/2 TRS PLPS MS	CMRCL	2800-20-0208	2
NONE	INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

WAVETEK PARTS LIST

TITLE: MODEL 23, 12MHZ SYNTHESIZEDFUNCTION GENERATOR

ASSEMBLY NO. 1000-00-0360

REV B

PAGE 1

2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. SEE 0004-00-0360 FOR INSTRUMENT SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 4/22/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR M.S. Mulk	4/22/85	TITLE: MODEL 23, 12 MHz SYNTHESIZED FUNCTION GENERATOR
FINISH WAVETEK PROCESS —	RELEASE APPROV D. Gish	4/22/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 23	DWG NO 1000-00-0360 REV B
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

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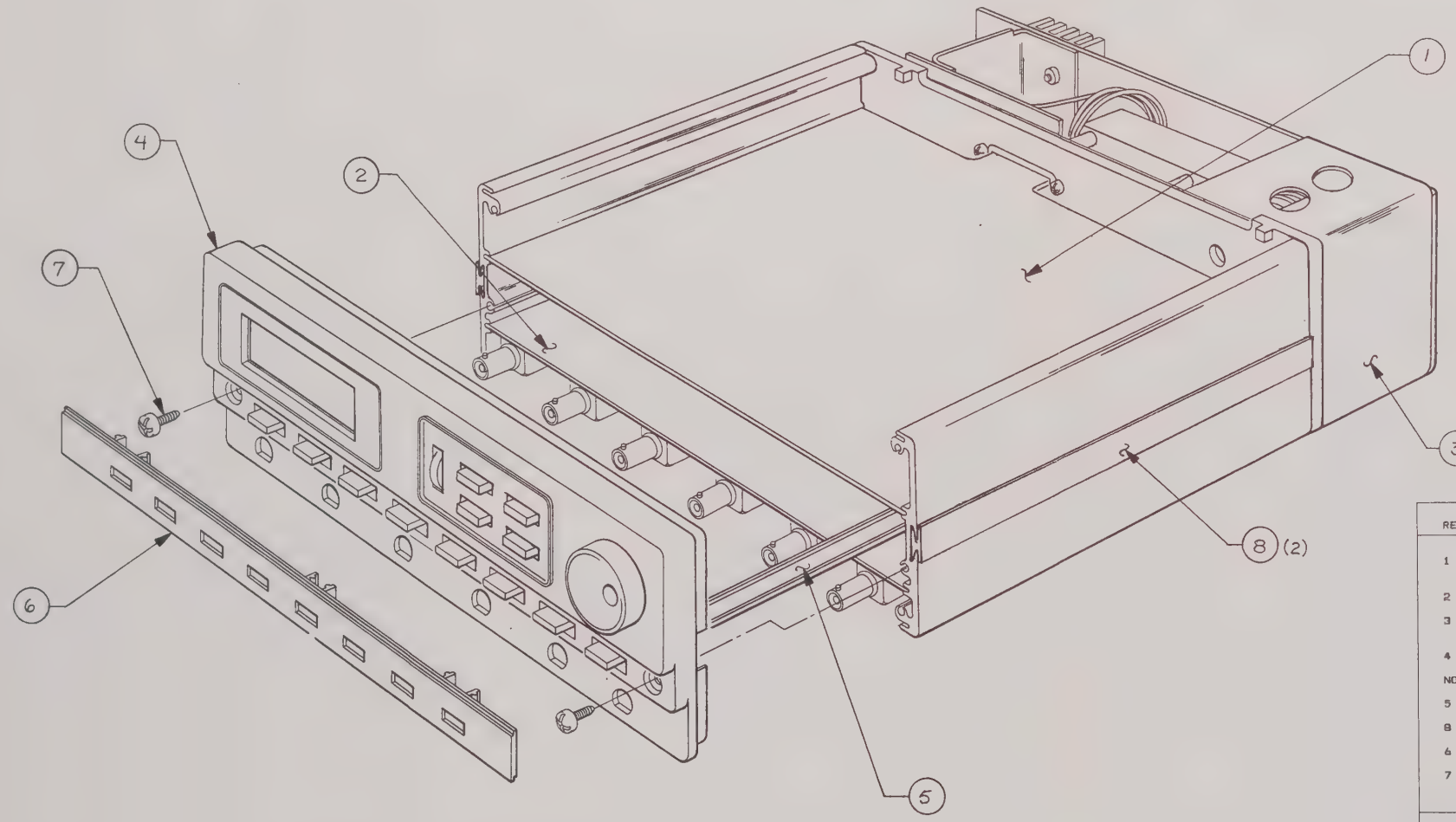
C	# 7459	JJ	9/25/86	A.R.T.



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, MPROC/SYNTHESIZER BD	23-1454	WVTK	1100-00-1454	1
2	PCA, WAVEFORM GEN BD	23-1455	WVTK	1100-00-1455	1
3	ASSY, REAR PANEL & POWER SUPPLY	23-1703	WVTK	1101-00-1703	1
4	ASSY, FRONT PANEL-23	23-1701	WVTK	1201-00-1701	1
NONE	ASSY, CABLE KIT-23	23-1705	WVTK	1207-00-1705	1
5	POWER ROD	21-6201	WVTK	1400-01-6201	1
8	INSERT, SIDE PANEL	20-7910	WVTK	1400-01-7910	2
6	BEZEL, KEY (MODEL 23)	23-8120	WVTK	1400-01-8120	1
7	SCREW, S/T TYPE B, P.H. CROSS RECESS, 8X1/2	8-18 X 5/8	CMRCL	2800-22-8910	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, CHASSIS-23	1101-00-1700	C
		PAGE 1	

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. SEE 0004-00-0360 FOR INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN AMY PALMADGE	DATE 4/19/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR M. F. Null	6/14/85	TITLE ASSEMBLY, CHASSIS
FINISH WAVETEK PROCESS —	RELEASE APPROV D. Fish	4/26/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 23	DWG NO. 1101-00-1700 REV C
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

1101-00-1700 C

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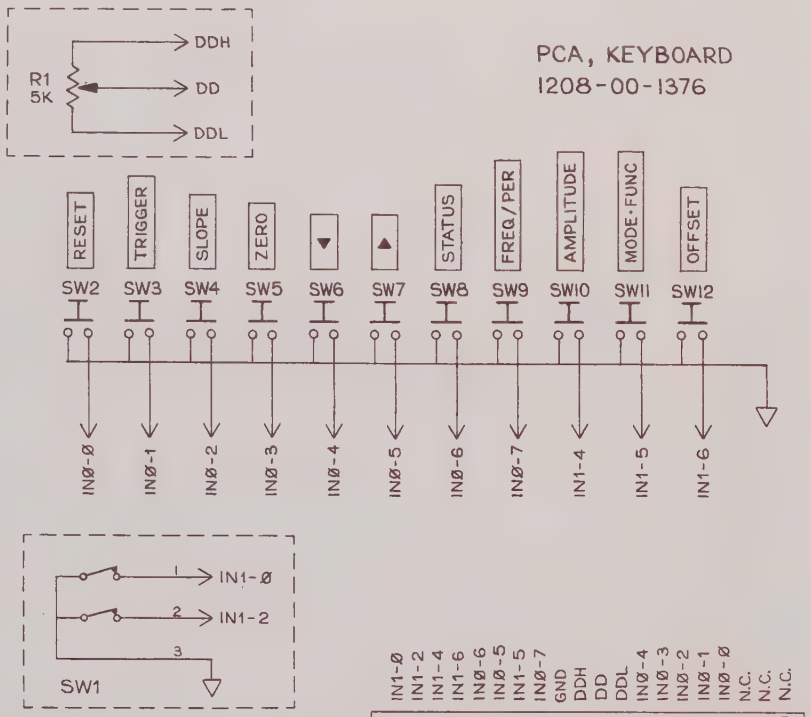
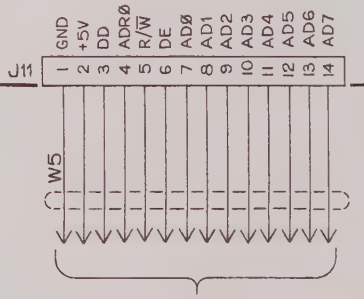
REV	ECN	BY	DATE	APP

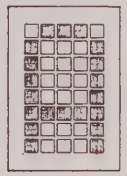
PCA, KEYBOARD
1208-00-1376



ASSEMBLY, FRONT PANEL
1201-00-1701

PCA, DISPLAY
1208-00-1874





DETAIL "A"

2. RESISTOR VALUES ARE IN OHMS.

1. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0360.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 3/21/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR	6/24/85	TITLE: SCHEMATIC, FRONT PANEL
FINISH WAVETEK PROCESS —	RELEASE APPROV	6/24/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± 010 ANGLES ± 1° .XX ± 030		
	DO NOT SCALE DWG		MODEL NO. 23 / DWG NO 0103-00-1701 / REV —
	SCALE —		CODE IDENT 23338 / SHEET 1 OF 1

0103-00-1701

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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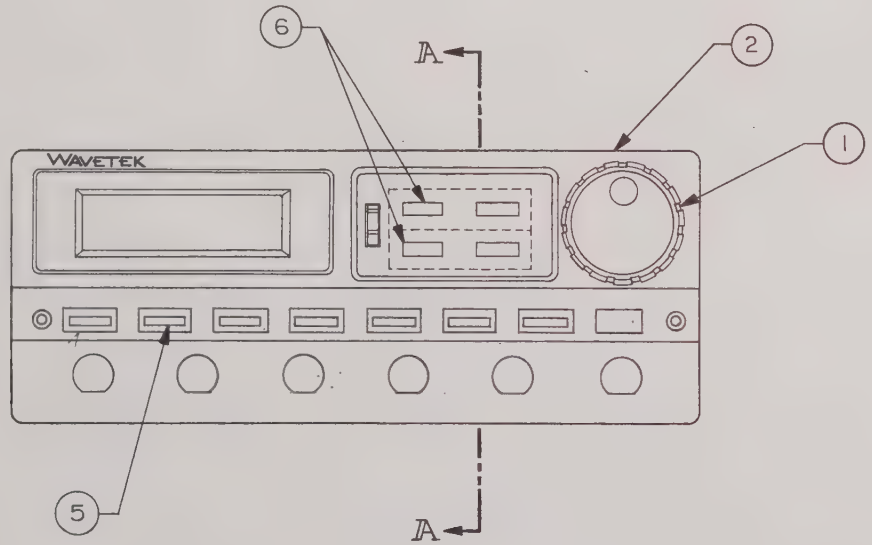
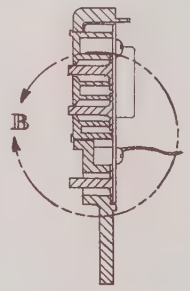
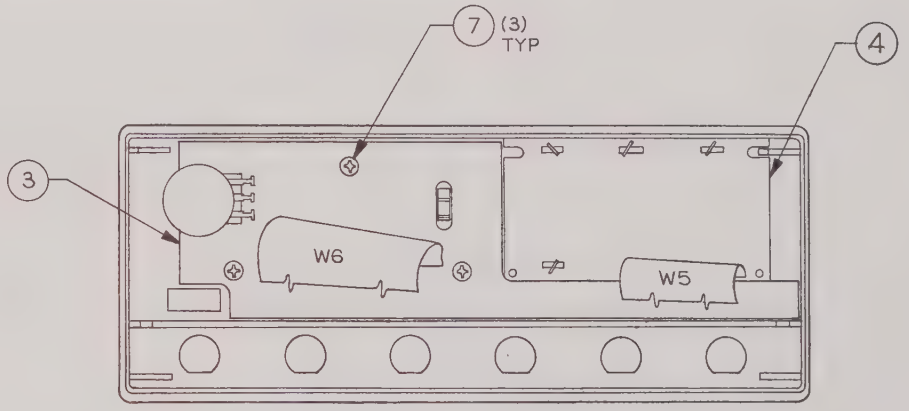
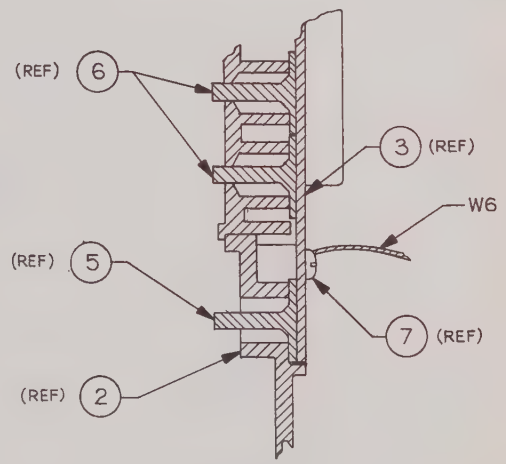
REV	ECN	BY	DATE	APP





SECTION A





DETAIL B
SCALE: 2/1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, FRONT PANEL	0103-00-1701	WVTK	0103-00-1701	1
1	ASSY ENCODER KNOB	23-1731	WVTK	1201-00-1731	1
2	FRONT HOUSING-23 SCREENED	23-8659	WVTK	1201-00-8659	1
3	PCA, KEYBOARD	23-1376	WVTK	1208-00-1376	1
4	PCA, DISPLAY BD	23-1874	WVTK	1208-00-1874	1
5	KEY PAD STRIP	21-6230	WVTK	1400-01-6230	1
6	KEYPAD STRIP MOD M/F: 1400-01-6230	1400-01-9409	WVTK	1400-01-9409	2
7	SCREW, S/T TYPE B, PAN CROSS RECESS, 4-24X1/4	4-24 X 1/4	CMRCL	2800-22-4142	3

WAVETEK PARTS LIST	TITLE: ASSY, FRONT PANEL-23	ASSEMBLY NO.: 1201-00-1701	REV
		PAGE 1	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: AMY TALMADGE	DATE: 1/7/84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR: M. S. Smith	4/26/85	TITLE: ASSEMBLY, FRONT PANEL - 23
FINISH: WAVETEK PROCESS	RELEASE APPROV: 4/26/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLES ±1°; XX ± .030		
	DO NOT SCALE DWG	MODEL NO.: 23	DWG NO: 1201-00-1701 REV: A
	SCALE: FULL & AS NOTED	CODE IDENT: 23338	SHEET 1 OF 1

1201-00-1701 A

BISHOP GRAPHICS, INC. CYPRESS REORDER NO. A27088

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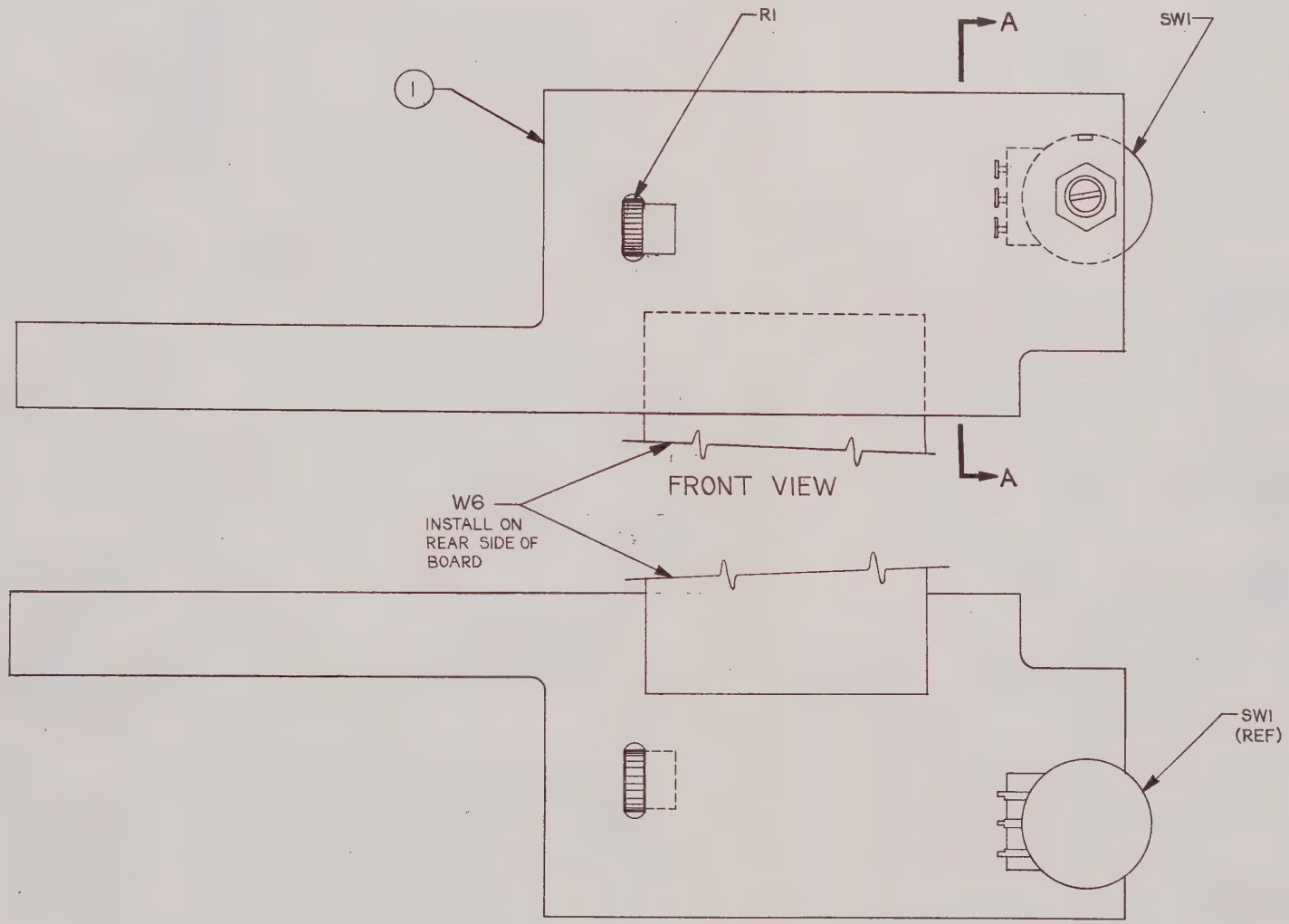
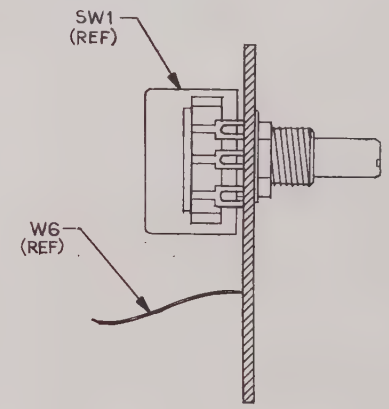
REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCB KEYBOARD	1700-00-1376	WVTK	1700-00-1376	1
R1	POT, 5K	4600-05-0211	WVTK	4600-05-0211	1
SW1	SWITCH, ROTARY CONDUCTOR	5104-00-0026	WVTK	5104-00-0026	1
W6	CABLE, FLEXIBLE FLAT 2", 20 PIN	1-88665-9	AMP	6001-60-0008	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, KEYBOARD	1208-00-1376	A
		PAGE 1	





SECTION A-A

1. SEE 0103-00-1701 FOR SCHEMATIC.

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 12/13/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR M.S. Muth	6/26/85	TITLE PCA, KEYBOARD BOARD
	RELEASE APPROV D.Fish	6/26/85	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 23/75	DWG NO. 1208-00-1376 REV A
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS-ACCUPRESS REORDER NO A2708

1208-00-1376 A

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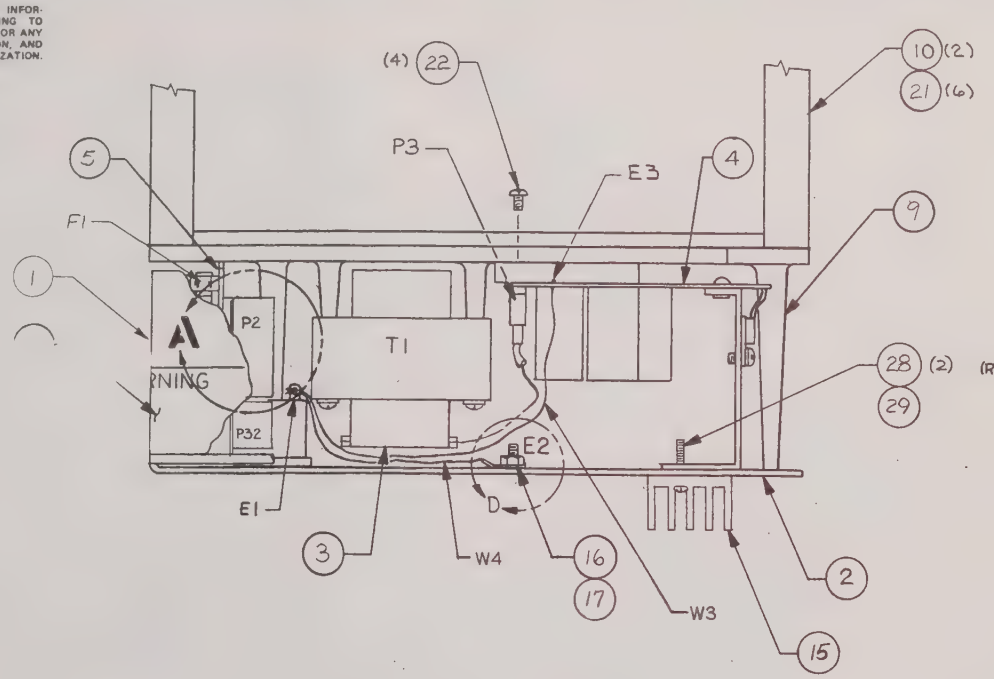
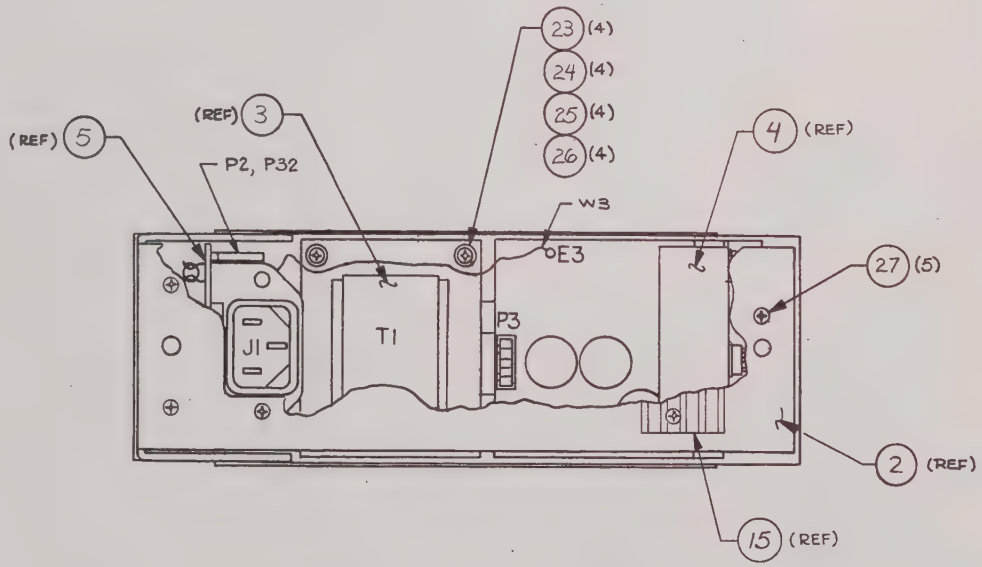
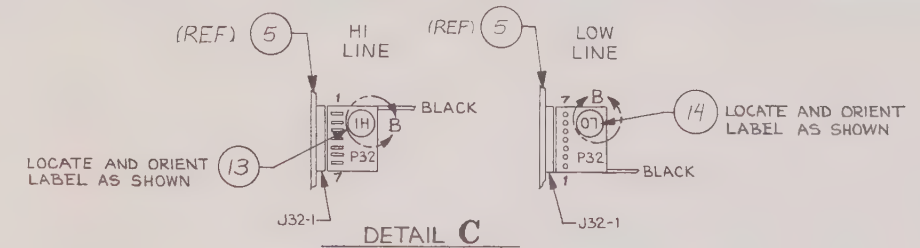
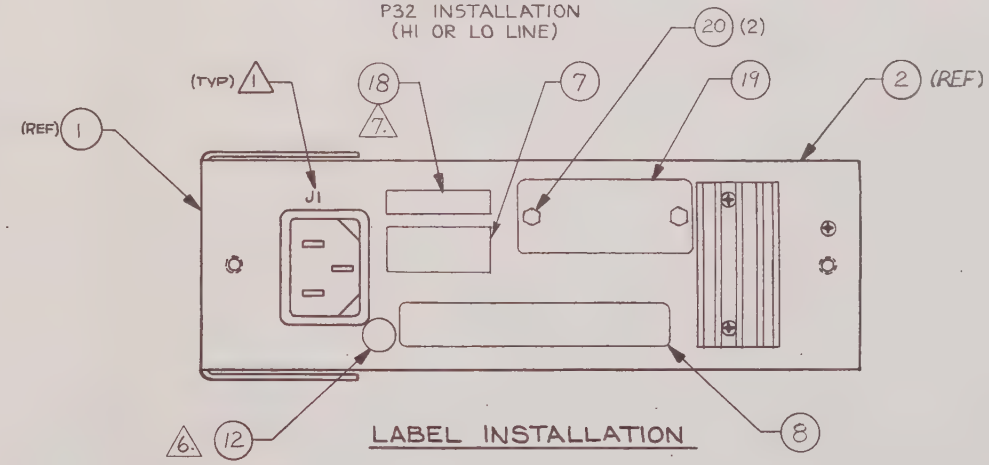
REV	ECN	BY	DATE	APP
B	#4882	DT	4/2/85	A.R.T.
C	#6080	AT	2/20/86	A.R.T.
D	#7495	DT	9/25/86	A.R.T.
E	#7999			J.C.T.
F	#9109	J.C. 7-28-87	9/25/87	A.R.T.



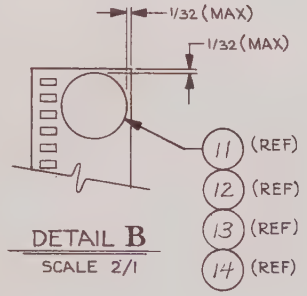




DETAIL C
P32 INSTALLATION (HI OR LO LINE)

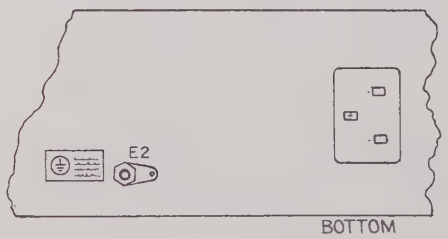


LABEL INSTALLATION

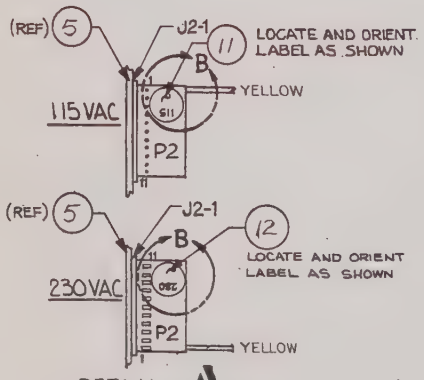


DETAIL B
SCALE 2/1

DETAIL B
SCALE 2/1



DETAIL D
MARK INSIDE OF REAR PANEL WITH SAFETY EARTH TERMINAL SYMBOL APPROXIMATELY AS SHOWN NEAR E2.



DETAIL A
P2 INSTALLATION (115VAC OR 230VAC)

DETAIL 'A' { 115 VAC / 230 VAC

WIRING LIST		
FROM	TO	REF DES
E1	E2	W4
E1	E3	W3
P2 (1 THRU 11)	J2 (1 THRU 11)	—
P2 (11 THRU 1)	J2 (1 THRU 11)	—
P3 (1 THRU 5)	J3 (1 THRU 5)	—
P32 (1 THRU 7)	J32 (1 THRU 7)	—
P32 (7 THRU 1)	J32 (7 THRU 1)	—

7. FOR 23-S-XXXX REPLACE ITEM 18 WITH OPTION LABEL P/N 1400-01-9990.
6. INSTALL ON UNITS SHIPPED IN 230 VAC CONFIGURATION ONLY.
5. P2 AND P32 NORMALLY ASSEMBLED SO THAT 115, HI LABELS NORMALLY APPEAR THROUGH FUSE COVER.
4. WIRES AND CABLES OBTAINED FROM CABLE KIT 1207-00-1705.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0360.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.

NOTE. UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1101-00-1703

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 3/7/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	4/24/85	TITLE ASSEMBLY, REAR PANEL AND POWER SUPPLY
FINISH WAVETEK PROCESS	RELEASE APPROV	6/26/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 23	DWG NO. 1101-00-1703 REV F
	SCALE 1/1 & NOTED	CODE IDENT 23338	SHEET 1 OF 1

1101-00-1703 F

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3361

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
3	TRANSFORMER	WVTK	23-1860	1204-00-1860	1
2	SUB ASSY, REAR PANEL	23-1906	WVTK	1206-00-1906	1
4	PCA, POWER SUPPLY	21-1118	WVTK	1208-00-1118	1
5	PCA, AC PRIMARY	21-1119	WVTK	1208-00-1119	1
8	I.D. LABEL	183-9110	WVTK	1400-00-9110	1
6	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
11	LABEL, 115 VAC	21-6900	WVTK	1400-01-6900	1
12	LABEL, 230 VAC	21-6910	WVTK	1400-01-6910	1
1	COVER, FUSE	1400-01-8183	WVTK	1400-01-8183	1
10	PANEL, SIDE-23 (GPIB)	23-8463	WVTK	1400-01-8463	2
13	LABEL, HI	1400-01-9420	WVTK	1400-01-9420	1
14	LABEL, LO	1400-01-9430	WVTK	1400-01-9430	1
15	HEATSINK, REAR PANEL	1400-01-9443	WVTK	1400-01-9443	1
19	COVER PLATE	23/75-9653	WVTK	1400-01-9653	1
7	LABEL, CAUTION	1400-01-9880	WVTK	1400-01-9880	1
18	LABEL, OPTION, MODEL 23	1400-01-9890	WVTK	1400-01-9890	1

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL & POWER SUPPLY | ASSEMBLY NO. 1101-00-1703 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
9	PANEL, POWER SUPPLY	1400-02-2080	WVTK	1400-02-2080	1
16	TAB, QUICK DISCONNECT	42822-4	AMP	2100-04-0045	1
F1	FUSE, 1/2A, 250V	313.500	LITFU	2400-05-0010	1
20	RIVET, SNAP, PLASTIC	SR 4050	RICH	2800-12-0046	2
17	NUT, FLEXLOCK, CAD I 6-32	6-32 NUT F.L.	CMRCL	2800-15-6100	1
21	SCREW, SELF TAPPING TYPE B, PAN CROSS	8-18 X 1/2	CMRCL	2800-22-8208	6
22	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	4
23	WASHER, FLAT, 6(.375 O.D.)	6 SAE FLAT WASHER	CMRCL	2800-26-6000	4
29	WASHER, SPLITLOCK, 4	MS35338-135	COML	2800-28-4000	2
24	WASHER, FLAT, FIBER, #6	MS35338-136	COML	2800-28-6000	4
28	SCREW, PAN, CAD I, CROSS RECESS,	MS51957-17	COML	2800-38-4108	2
26	WASHER, SPLIT LOCK #6 6	#6SRLW	CMRCL	2800-42-6000	4
27	SCERW, F.H. 100 DEG CSK, CROSS RECESS4-40X3/8	4-40X3/8 F.H.	CMRCL	2800-44-4106	5

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL & POWER SUPPLY | ASSEMBLY NO. 1101-00-1703 | REV F

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST REAR PANEL ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		O 23 | DWG NO 1101-00-1703 | REV F
	SCALE		CAGE CODE 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A21080

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REV	ECN	BY	DATE	APP
C	#4916	DT	7/10/85	A.R.T.
D	#4929	DCT	10/9/85	A.R.T.
E	#6080	DT	1/14/86	A.R.T.
F	#7644	A.T.	8/27/86	J.M.

STANDBY

R1 3.92K, R2 357K, R4 4.87K, U1A LM393

MICROPROCESSOR

U3 6303 — STBY, Vcc, NMI, EXTAL, 3.072 MHz E4, E5, R8 100K, R7 KW1 100K, R9 KW2 100K, BLOAD, BTST, RESET, P10 DATA, P11 CLK, P12 KNOB INTERRUPT, P13 AMP, P14 OFST, P15 FRQ, P16 XY, P17 KM, Vss, IRQ, AS, R/W, E, A0–A15 ADR0–ADR15, D0–D7 AD0–AD7

RESET

U2 REF, CT, RESET; C1 .01, C2 10/25V; R5 10K; TL7705A

BATTERY TEST

CR1 FD777, R6 1M, Q1 VN10KM, C3 .1, ON, MR

R10 30.1K, R12 3.16K, C4 .1, R15 20K, CR2 MBR120, CR3 HP2811, R11 2K, BT1 BR2/3A, U1B LM393, BTST, R13 2.37K, R14 301K

CLOCK

U4 74LS74; E8 6.144 MHz (2B8), E9, E6 3.072 MHz, E7; R16 10K, C6 .1, IRQ

U20 74LS00, U21 74AS08

ADDRESS LATCH

U5 74HC373 — AD0–AD7 → ADR0–ADR7; C7 .1

ADDRESS DECODER

U8 74HC138 — ADR15, ADR14, ADR13; C8 .1, R17 49.9K

U21 74AS08; U19 74HC04

U9 MC1 4066B — COMM, DISP, RAM, MR; R18 49.9K; BBV

I/O

MEMORY

U6 27128-45 — C9 .1; ADR0–ADR13, AD0–AD7, CE, OE, RD

U7 6116LP-2 — AD0–AD7, ADR0–ADR10, RAM, RD, R/W, BE; C10 .1, BBV

U18 74HC86; U20 74LS00; U19 74HC04

R19 3.01K, R20 3.01K, Q2 2N3904 (2), Q3, C89 .1, C90 .1, C91 .001, ON

ANALOG/PANEL DECODER

U10 74HC138 — ADR2, ADR1, ADR0, BE, G2B, G2A; CLK1, CLK2, CLK3, BEN1, BEN2, RKIRQ

U19 74HC04 — ADR12

DATA LATCH

U11 74HC373 — AD0–AD7 → LAD0–LAD7; C11 .1

ANALOG INTERFACE

U12 74HC374 — CLK1; ÷100, FR4, FR5, FR6, FR7, OVRNG → LAD0–LAD7; C12 .1

U13 74HC374 — CLK2; FSI, FSØ, KILL, TRT, SQR, SIN, LF → LAD0–LAD7; C13 .1

U14 74HC374 — CLK3; HAV, MCI, MCØ, SYNTH, TRIG SLOPE, TRIGEN, SB, SA → LAD0–LAD7; C15 .1

FRONT PANEL INTERFACE

U15 74HC244 — (J12-17) INØ-Ø, (J12-16) INØ-1, (J12-15) INØ-2, (J12-14) INØ-3, (J12-13) INØ-4, (J12-6), (J12-5), (J12-8); INØ-6, INØ-5, INØ-7; BEN1; C14 .1

U16 74HC244 — IN1-Ø, IN1-2, (J12-3) IN1-4, (J12-7) IN1-5, (J12-4) IN1-6, IN1-7; BEN2; C15 .1

RN1 470K, RN2 470K

E35, E36, E38, E39; JP2, JP1, E34, E37; R25 10K, R26 10K

KNOB INTERRUPT, R27 3.32K, Q4 2N3904, IRQ

U19 74HC04; U21 74AS08; C16 .1; DISP, DE

R21 221K, R22 221K, R23 15K, R24 3.57K; KW1, KW2, (J12-1), (J12-2), (J12-12) DDL, (J12-10) DDH

U17 74HC10; U18 74HC86; U19, 74HC04; RKIRQ, KM

C17 10/25, C18 10/25, C19 .1, C20 10/25, FB1

J6 ANALOG BOARD

FR7, SYNTH, OVRNG, FR4, FR6, FR5, GND, VNULL, VAMP, VFREQ, VOFST, GND, LF, SIN, TRI, AØ, A1, KILL, MCØ, ÷100

J10 DISPLAY

GND, +5V, DD, ADR Ø, R/W, DE, ADØ, AD1, AD2, AD3, AD4, AD5, AD6, AD7

P4 EDGE CONNECTOR

TRIG EN	1A	1B	GND
FSØ	2A	2B	GND
TRIG SLOPE	3A	3B	
MCI	4A	4B	
-15V	5A	5B	GND
+5V	6A	6B	GND
+5V	7A	7B	SQR
+15V	8A	8B	LF
HAV	9A	9B	GND
FS1	10A	10B	GND

J8 / J9 / J14

J8 F/G SYNC (2A4) → J9 SYNC (2A4) → J14 FSYNTH (2A2)

J12 KEYBOARD

IN1-Ø (CPRE 1), IN1-2 (CPRE 2), IN1-4 (PB9), IN1-6 (PB11), INØ-6 (PB7), INØ-5 (PB6), IN1-5 (PB10), INØ-7 (PB8), GND, DDH, DD, DDL, INØ-4 (PB5), INØ-3 (PB4), INØ-2 (PB3), INØ-1 (PB2), INØ-0 (PB1)

J16 COMM BOARD

GND, +5V, +15V, -15V, R/W, E, IRQ, MR, AD4, AD5, AD6, AD7, ADRØ, ADR1, ADR2, COMM, ADØ, AD1, AD2, AD3

5. * INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
4. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0360.
3. JP1, JP2 SHOWN IN 50Ω OUTPUT IMPEDANCE SELECTION POSITIONS.
2. CAPACITOR VALUES ARE IN MICROFARADS (μF).
1. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN AMY TALMADGE 9/28/84 | PROJ ENGR 6/26/85 | RELEASE APPROV 6/26/85 | TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC, MICROPROCESSOR/ SYNTHESIZER BOARD

MODEL NO 23 | DWG NO 0103-00-1454 | REV F | CODE IDENT 23338 | SHEET 1 OF 2

0103-00-1454 F

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3864

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REV	ECN	BY	DATE	APP

SAMPLE AND HOLD

U32 DAC1006 — LAD0–LAD7 (1D2), CS (1D4), ADR0 (1D5), WR, XFER, VREF, RFB, IOUT1, IOUT2

U33A LF353 — U33B LF353

U18 74HC86 — E (1C6)

U34A DG211 — U34B DG211 — U34C DG211 — U34D DG211 — (1C7) AMP, OFST, FRQ, XY

U35A TL084 — VAMP (J6-9)

U35B TL084 — VOFST (J6-11)

U35C TL084 — VFREQ (J6-10)

U35D TL084 — VNULL (J6-8)

FREQUENCY SYNTHESIZER

U22 MC145155 — (1C7) CLK, (1C7) DATA, (1D) EN, 6.144 MHz (1B6), Y1 6.144 MHz

U23A LF353 — U23B LF353

U24 74F151 — U25 74HC161 — U26 74F74 — U27 74F151

U28 74HC390 — U29 74HC390

U30 74HC02 — U31 74HC32

FR4 (14C), FR5 (14C), FR7 (14C), FR6 (14C)

SB (1C2), SA (1C2), J9 (1B6) SYNC, J8 (1B6) F/G SYNC, E14, E15

J14 FSYNTH — E12, E13

SYNTH (12C)

Q5 2N3563 (2), Q6, Q7 2N3563, Q8 2N3563, Q9 2N5771, Q10 2N3563, Q11 2N3904

CR4–CR8 BB909B(5), CR9 IN751A, CR10 HP2811, CR11 IN4148, CR12 IN4148

FB2, FB3, FB4

(2A2) E12, E13 — E14, E15 (2A4)

(2BB) E10, E11 — E8, E9 (1B6)

(1B6) E6, E7 — E4, E5 (1D7)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN AMY TALMADGE	DATE 12/10/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	4/26/85	TITLE: SCHEMATIC, MICROPROCESSOR/ SYNTHESIZER BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV 6/26/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 23 / DWG NO 0103-00-1454 / REV F
	SCALE		CODE IDENT 23338 / SHEET 2 OF 2

0103-00-1454 F.

BISHOP GRAPHICS ACC. PRESS RECORDER NO. A2706

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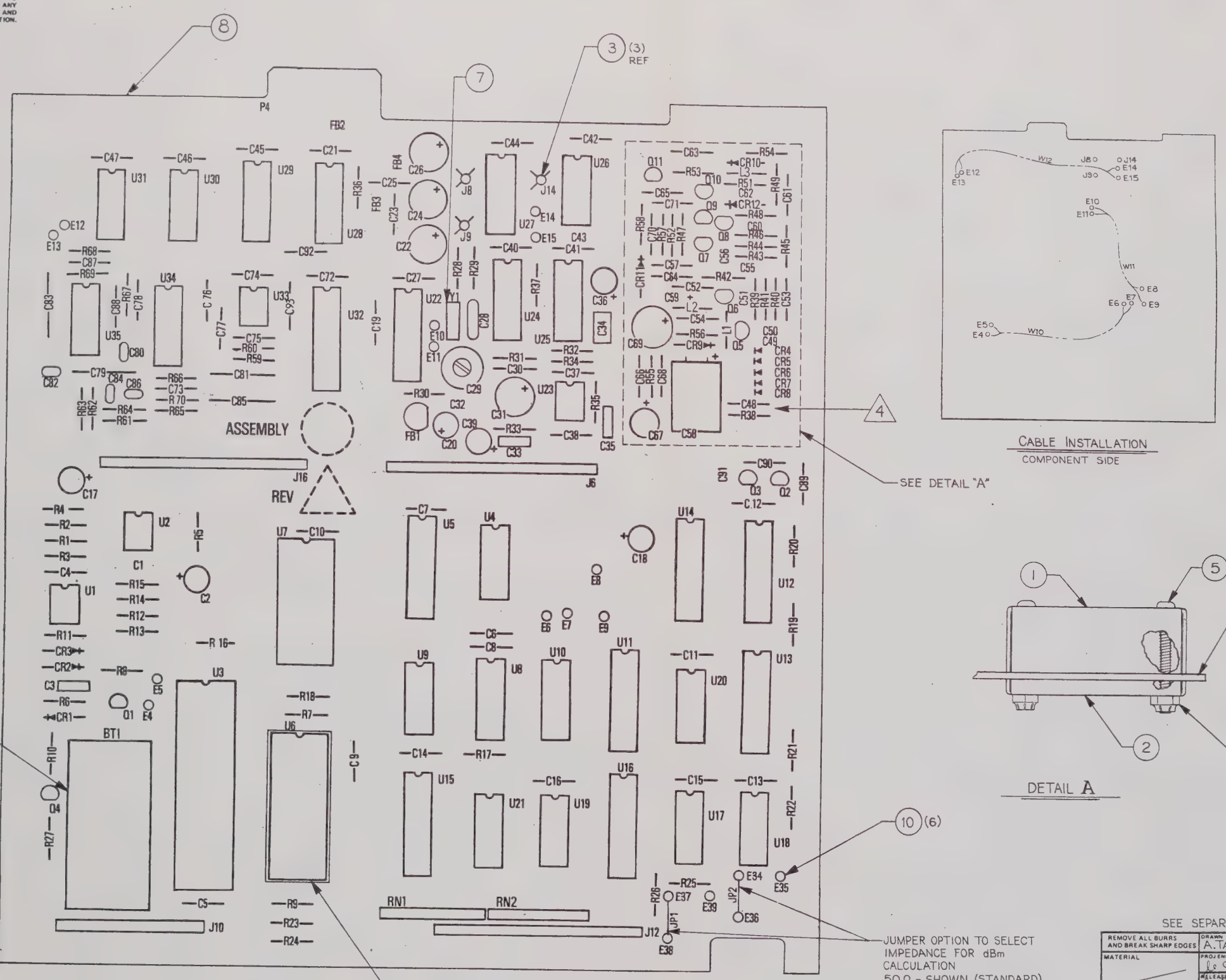
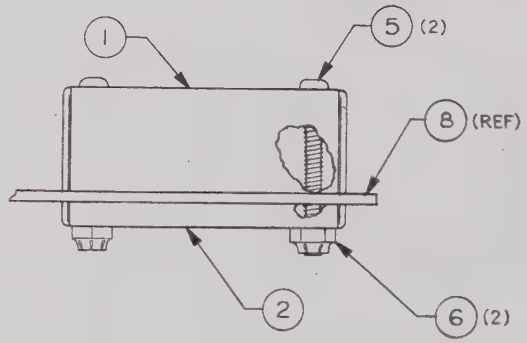
REV	ECN	BY	DATE	APP
C	#4916			
D	#4982	JJT	12/20/85	A.R.T.
E	#7376	JJT	4/30/86	A.R.T.
F	#7644	A.C.T.	8/27/86	YM
G	#9109	M.C. 9-10-87	9-11-87	H.N.



CABLE INSTALLATION
COMPONENT SIDE

CABLE HOOKUP LIST		
REF DES	DESTINATION FROM	TO
W10	E6	E4
	E7 ⏚	E5 ⏚
W11	E10	E8
	E11 ⏚	E9 ⏚
W12	E12	E14
	E13 ⏚	E15 ⏚



DETAIL A

NOTE UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-1454

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 12/5/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	4/24/85	TITLE: PCA, UPROC / SYNTHESIZER BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV	4/26/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1° XX : 030		
	DO NOT SCALE DWG	MODEL NO 23	DWG NO 1100-00-1454 REV G
	SCALE 2/1 & AS NOTED	CODE IDENT 23338	SHEET 1 OF 1

1100-00-1454 G

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC MPROC/SYNTHESIZER BD	0103-00-1454	WVTK	0103-00-1454	1
1	SHIELD, VCO, TOP	23-8633	WVTK	1400-01-8633	1
2	SHIELD, VCO, BOTTOM	23-8643	WVTK	1400-01-8643	1
C80 C82 C84 C86	CAP, CER, MON, .001MF, 100V, RADIAL LEAD	5018EM100RD102M	KYCRA	1500-00-1706	4
C55	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C91	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	1
C1 C43 C49 C50 C51 C56 C60 C62	CAP, CER, MN, .01MF, 50V Z5U, +80/-20% RAD LEAD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	8
C10 C11 C12 C13 C14 C15 C16 C19 C21 C23 C25 C27 C30 C37 C38 C4 C40 C41 C42 C44 C45 C46 C47 C5 C52 C53 C54 C57 C6 C61 C63 C64 C65 C66 C68 C7 C70 C71 C72 C73 C74 C75 C76 C77 C78 C8 C87 C88 C89 C9 C90 C92	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	52
C93	CAP, CER, MON, .47UF, 20%, 50V, Z5U	CRC23OZ5U474M050	CORNG	1500-04-7406	1
C28	CAP, MICA, 20PF, 500V	DM15-200J	ARCO	1500-12-0000	1

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J12 J16 J6	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0151	3
J10	HEADER CONNECTOR, 14 PIN	643114-1	AMP	2100-02-0161	1
3	COAX SOCKET	226287-2	AMP	2100-03-0038	3
J14 J8 J9	SPRING SOCKET	50935-1	AMP	2100-03-0039	3
10	SOCKET, MINISERT	75060-012	BERG	2100-03-0076	6
9	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
Y1	CRYSTAL, 6.144 MHZ	MP-1	MTRON	2300-00-0014	1
7	TRANSIPAD, CRYSTAL	311-200	BIVAR	2800-11-0023	1
6	LOCK NUT	21FA-440	SPS	2800-16-0004	2
5	SCREW, PAN, CAD I 4-40 X1	4-40 X1 PAN	CMRCL	2800-38-4116	2
4	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
FB2 FB3 FB4	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	3
FB1	BALUN CORE	2873000902	FARIT	3100-00-0002	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
R51	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R10	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R14	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R12	RES, MF, 1/8W, 1%, 3.16K	RN55D-3161F	TRW	4701-03-3161	1
R47	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	1
R27	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R24	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R2	RES, MF, 1/8W, 1%, 357K	RN55D-3573F	TRW	4701-03-3573	1
R1	RES, MF, 1/8W, 1%, 3.92K	RN55D-3921F	TRW	4701-03-3921	1
R4	RES, MF, 1/8W, 1%, 4.87K	RN55D-4871F	TRW	4701-03-4871	1
R35	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R17 R18 R28 R29	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	4
R48 R49	RES, MF, 1/8W, 1%, 49.9	RN55D-49R9F	CORNG	4701-03-4999	2
R60	RES, MF, 1/8W, 1%, 6.04K	RN55D-6041F	MEPCO	4701-03-6041	1
R63 R68	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	2
R59	RES, MF, 1/8W, 1%, 8.87K	RN55D-8871F	TRW	4701-03-8871	1
RN1 RN2	RES MODULE, 470K	810-1-474-J	TRW	4770-00-0034	2

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C17 C18 C2 C20 C36 C39 C67	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	7
C22 C24 C26 C31 C69	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	5
C58	CAP ELECT, END MOUNT, 0.2 LEAD SPACE, 1000 MF	UVH1C102M	NICHC	1500-31-0214	1
C3 C35	CAP, POLY, .1MF, 63V, RADIAL LEAD	168/.1/J/63/B	WEST	1500-41-0813	2
C79 C81 C83 C85	CAP, POLY, .1MF, 50V, AXIAL LEAD	Z5A104M	ELPAC	1500-41-0823	4
C33	CAP, MET, POLY, 5% .033MF, 63V RADIAL LEAD SP .2	168/.033/J/63/A	WEST	1500-43-3304	1
C32 C34	CAP, MET-POLY, 5% .47MF, 63V RADIAL LEAD SP .2	168/.47/J/63/F	WEST	1500-44-7413	2
C29	VARI, 15-60PF, 200V	538-011F1560	ERIE	1500-56-0010	1
C59	CAP, TANT, 22MF, 20V	202A2002226M3	MATSO	1500-72-2621	1
8	DRILL DRWG, MPROC/SYNTHESIZER BD	1700-00-1454	WVTK	1700-00-1454	1
L3	CHOKE, 68 MICRO HENRY	IR-2	DALE	1800-00-0018	1
L1 L2	INDUCTOR, .1 MICRO H	1025-94	DELVN	1800-00-0020	2

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R16 R25 R26 R32 R5 R57 R61 R65 R66 R70	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	10
R7 R8 R9	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	3
R6	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	1
R52	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	1
R30	RES, MF, 1/8W, 1%, 11K	RN55D-1102F	TRW	4701-03-1102	1
R36 R37 R44 R45	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	4
R23	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R42 R53	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	2
R11 R31 R38 R40 R43 R46 R64 R69	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	8
R15 R58	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	2
R55 R56	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	2
R21 R22	RES, MF, 1/8W, 1%, 221K	RN55D-2213F	TRW	4701-03-2213	2
R13	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R34 R54	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R33	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R19 R20 R3 R39 R41 R62 R67	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	7

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
JP1 JP2	RESISTOR, 0 OHM JUMPER	JP02T68Q	ROHM	4799-00-0087	2
CR9	DIODE	1N751A	FAIR	4801-01-0751	1
CR2	DIODE	MBR 120	MOT	4806-02-0120	1
CR1	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	1
CR11 CR12	DIODE	1N4148	FAIR	4807-02-6666	2
CR10 CR3	DIODE	5082-2811	HP	4809-02-2811	2
CR4 CR5 CR6 CR7 CR8	DIODE, BB909B	5130-30395	AMPRX	4899-00-0040	5
Q10 Q5 Q6 Q7 Q8	TRANS	2N3563	FAIR	4901-03-5630	5
Q11 Q2 Q3 Q4	TRANS	2N3904	FAIR	4901-03-9040	4
Q9	TRANS	2N5771	NSC	4901-05-7710	1
Q1	TRANS	VN10KM	SILX	4902-00-0100	1
U35	IC	TL084CN	TI	7000-00-8400	1
U23 U33	IC	LF353N	NSC	7000-03-5300	2
U1	IC	LM393N	NSC	7000-03-9300	1
U32	IC, DAC	DAC1006LCN	NAT	7000-10-0600	1
U2	IC, RESET GEN	TL7705A	TI	7000-77-0501	1

WAVETEK PARTS LIST — TITLE: PCA, MPROC/SYNTHESIZER BD — ASSEMBLY NO. 1100-00-1454 — REV G — PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MPROC/SYNTHESIZER BD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 23 — DWG NO 1100-00-1454 — REV G
	SCALE		CODE IDENT 23338 — SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27085

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U34	CMOS, SW, QUAD ANALOG	DG211CJ	SILX	8000-02-1100	1
U7	IC, CMOS, 2KX8 STATIC RAM	HM6116LP-2	HTACH	8000-61-1602	1
U3	IC, CMOS 8 BIT MCU	HD6303R	HTACH	8000-63-0300	1
U20	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U30	GATE NOR QUAD A-INPUT	MM74HC02N	NSC	8000-74-0240	1
U19	CMOS, ENVERTER, HEX	MM74HC04	NSC	8000-74-0440	1
U21	GATE NAND QUAD 2-INPUT POS	SN74AS08N	TI	8000-74-0820	1
U17	GATE, NAND, 3 INP, CMOS	MC74HC10N	MOT	8000-74-1040	1
U31	GATE, OR, QUAD 2-INPUT	MM74HC32N	NSC	8000-74-3240	1
U26	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	1
U4	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	1
U9	BILATERAL SWITCH, QUAD ANALOG, CMOS	CD4066BE	RCA	8001-40-6600	1
U10 U8	DECODER, 3-8 LINE,	MC74HC138N	MOT	8007-41-3840	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO	REV
	PCA, MPROC/SYNTHESIZER BD	1100-00-1454	G
		PAGE 7	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	CMOS				
U24 U27	IC, 8-INPUT MULTIPLEX	74F151PC	FAIR	8007-41-5120	2
U25	COUNTER, PROG 4B BIN, CMOS	MC74HC161N	MOT	8007-41-6140	1
U15 U16	OCTAL TRI-STATE BUFFER	MM74HC244N	NSC	8007-42-4440	2
U11 U5	LATCH, OCTAL TRANSPAR W/3 STATE, CMOS	SN74HC373N	TI	8007-43-7340	2
U12 U13 U14	CMOS, D-F/F, TRI-S OCT	74HC374	TI	8007-43-7440	3
U28 U29	COUNTER, DUAL 4B BCD, CMOS	MM74HC390N	NSC	8007-43-9040	2
U18	GATE XOR, QUAD 2 INP, CMOS	MC74HC86N	MOT	8007-74-8640	1
U22	CMOS, SYNTH, PLL FREQ	MC145155	MOT	8100-00-0007	1
U6	IC, PROGRAMMED EPROM V1.3, REF: 8004-82-7450	8600-00-0292	WVTK	8600-00-0292	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, MPROC/SYNTHESIZER BD	1100-00-1454	G
		PAGE 8	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MPROC/SYNTHESIZER BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG		
	SCALE		23 | 1100-00-1454 | G
			CODE IDENT 23338 SHEET 2 OF 2

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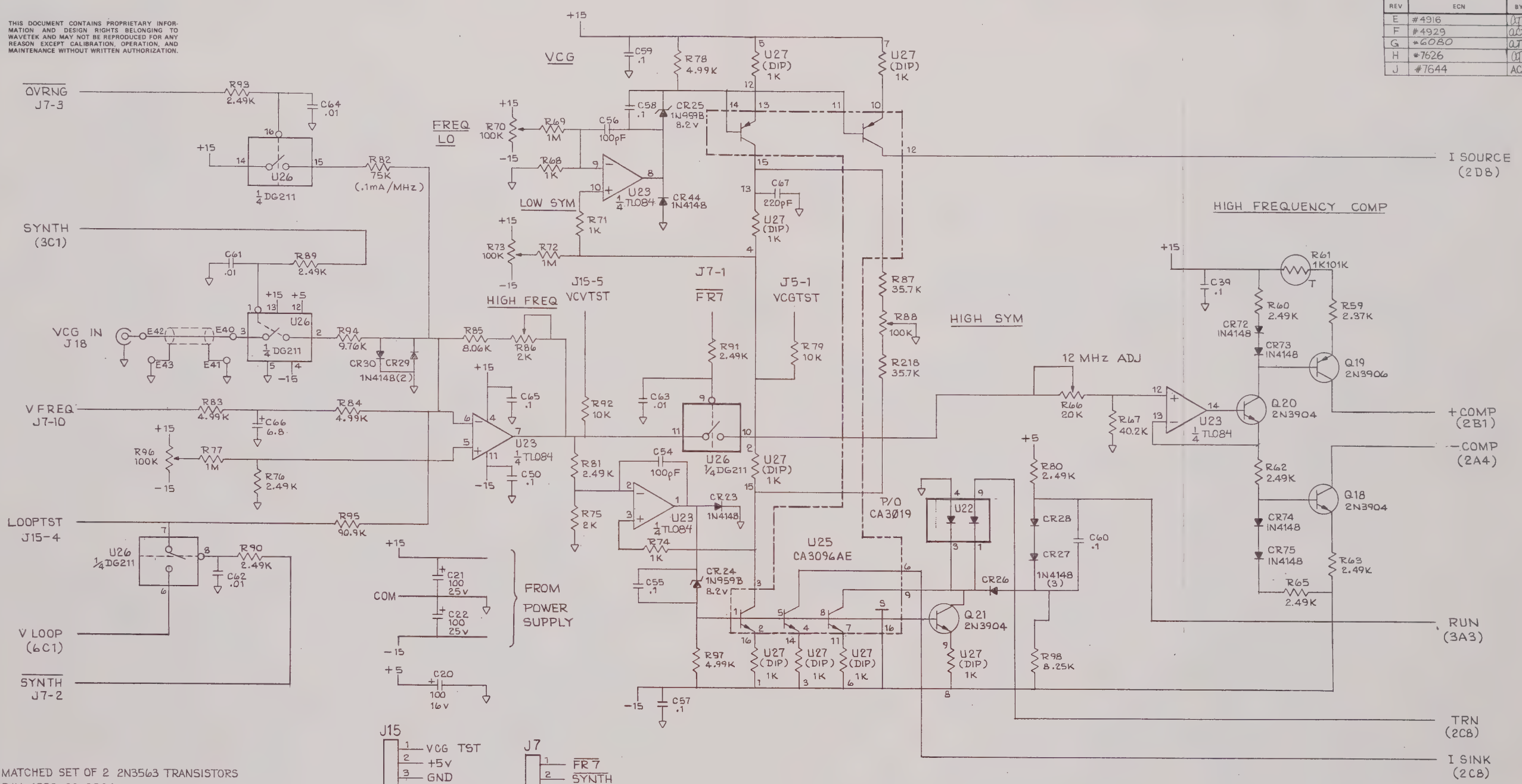
REV	ECN	BY	DATE	APP
E	#4916	DT	7/10/86	A.R.T.
F	#4929	ACT	10/8/86	A.R.T.
G	*6080	DT	1/10/84	A.R.T.
H	*7626	DT	7/24/86	A.R.T.
J	#7644	ACT	8/27/86	TM



8. MATCHED SET OF 2 2N3563 TRANSISTORS P/N 4998-00-0004.
7. MATCHED SET OF 6 FD-777 DIODES P/N 4898-00-0021.
6. * INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
5. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0360.
4. MATCHED PAIR FETS P/N 4998-00-0009 (SH 2 OF 6).
3. MATCHED PAIR CAPACITORS P/N 1509-80-0012 (SH 2 OF 6).
2. CAPACITOR VALUES ARE IN MICROFARADS (μF).
1. RESISTOR VALUES ARE IN OHMS (Ω), 1/8 WATT.

NOTE UNLESS OTHERWISE SPECIFIED

J15 — TEST: 1 VCG TST, 2 +5V, 3 GND, 4 LOOP TST, 5 VCV TST, 6 FUNC TST, 7 -15V, 8 -15V, 9, 10 RUN TST, 11, 12, 13 TRI TST, 14 +15V

J7 — DIGITAL BOARD: 1 FR7, 2 SYNTH, 3 OVRNG, 4 FR4, 5 FR6, 6 FR5, 7 GND, 8 VNULL, 9 VAMP, 10 VFREQ, 11 VOFST, 12 GND, 13 LF; 14 SIN, 15 TRI, 16 AØ, 17 AT, 18 KILL, 19 MCØ, 20 ÷1ØØ

P5 — EDGE CONNECTOR: TRIG EN 1A, FSØ 2A, TRIG SLOPE 3A, MC1 4A, -15V 5A, +5V 6A, SQR 7A, +15V 8A, HAV 9A, FS1 10A; 1B GND, 2B GND, 3B, 4B, 5B GND, 6B GND, 7B GND, 8B LF, 9B GND, 10B GND

J18 — VCG IN
J19 — TRIG IN
J20 — AM IN
J21 — TTL OUT
J22 — ECL OUT
J23 — FUNC OUT

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Jennie Coletta 12/6/84	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR Ken Kasaki 6/26/85	TITLE	SCHEMATIC, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV [illegible] 6/26/85	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030	
	DO NOT SCALE DWG	MODEL NO 23	DWG NO 0103-00-1455 REV J
	SCALE	CODE IDENT 23338	SHEET 1 OF 6

0103-00-1455 BJ

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

TRI COMP (2A4)
I SOURCE (1D1)
ISINK (1B1)
TRN (1B1)

CURRENT SWITCH

+15
R21 6.98K
Q5 2N5462
C36 .1
R12 15.8K
CR11 CR13 CR10 CR12 FD777 (4)
R22 0Ω
D G S
Q4 2N5485
C23 .1
R13 6.98K
-15

FREQUENCY RANGE SWITCHES

C37 3.5/13pF — 1MHz ADJ BOD
C25 *
C38 7/35pF — 1MHz ADJ TOD
C26 * SM
C29 820pF SM
C28 .01 1% MYLAR (3)
C24 *
C27 .1 1% MYLAR (3)
+5

Q1 2N3906 — R16 2.49K — C34 .001
Q2 2N3906 — R15 2.49K — C33 .001
Q3 2N3906 — R14 2.49K — C32 .001

R11 90.9
R20 90.9
R17 90.9

CR5 1N5282 — R4 7.5K — R5 10M — CR8 1N5282 — R9 20K
CR3 1N5282 — R7 10M — CR6 1N5282 — R19 20K
CR4 1N5282 — R6 10M — CR7 1N5282 — R18 20K

R8 7.5K
-15
C35 .1

FR6 J7-5
FR5 J7-6
FR4 J7-4

+15
C31 .1
R24 1K ½W
Q6 2N5485 (4)
R23 100
C30 .1
CR9 1N4143
Q9 2N3906
CR14 FD777
Q7 2N5485 (4)
R25 40.2
R26 100
TRIG BL
C40 .1
-15

+COMP (1C1)
TRITST J15-13
TRI (4C8)

(2A7) A B (2A7)
U22 P/O CA3019
Q12 2N3563 (2) (8)
Q13 (8)
R51 10K
R52 332
C46 330pF SM
R30 3.01K
R48 332
R50 100
R31 4.32K
Q8 2N3904
R28 1.1K
R29 10.5K
C42 .1
C41 .1
-15

-COMP (1C1)
5WSQR (3D2)
TRICOMP (2D8)

+15
C44 .1
R39 6.19K
R40 499 ¼W
R54 2K
R56 2K
R41 1.78K
R43 1.5K
C45 .1
CR18 HP2811
CR19 HP2811
Q15 2N5771
R53 33.2
R55 33.2
Q14 2N5771
CR58 FD777
CR57 FD777
A B (2B4) (2B3)
R47 100
Q16 2N3563
R42 332
CR21 1N4148
R44 4.7 ½W
+5
R32 4.7 ½W
C47 .1
Q11 2N3563
R37 100
CR17 1N4148
R38 332
R33 4.7 ½W
R36 10
R46 10
CR20 1N4148
R45 4.7 ½W
C49 5pF
5WSQR
R34 4.7 ½W
CR16 1N4148
Q10 2N5771
R49 100
R58 100
Q17 2N5771
CR15 1N4740
R35 2.49K
R57 4.64K
CR22 1N4740
C43 .1
-15
C48 .1

NOTE UNLESS OTHERWISE SPECIFIED
(SEE SHEET 1.)

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Jeniefatta	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Kurt Loomis	6/26/85	TITLE: SCHEMATIC, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV Bill 6/26/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 23 — DWG NO 0103-00-1455 — REV U
	SCALE		CODE IDENT 23338 — SHEET 2 OF 6

0103-00-1455 U

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3884

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REV	ECN	BY	DATE	APP

MODE	MCØ	MC1
SYNTH	Ø	1
CONT	Ø	1
TRIG	1	Ø
GATE	1	1

[MFSQ]
LF P5-8B
FSØ P5-2A
FS1 P5-10A
LF LEVEL
MCØ J7-19
MC1 P5-4A
TRIG SLOPE P5-3A
TRIG IN J19
HAV P5-9A
SWSQR (1A4)
SYNTH (1B8)
SYNTH (1D8)
SQUARE SELECTOR
HFSQ (6D8)
FGSYNC P8
BOTTOM
SYNTH SIG (4D8)
RUN (1B1)
RUNTST J15-10
KILL (J7-18)
TRIG EN P5-1A
TRIGGER LOGIC
TTLSQR (4A8)
SQR P5-7A
÷100 J7-20

NOTE: UNLESS OTHERWISE SPECIFIED
(SEE SHEET 1.)

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Jennie Potts	DATE 6/26/85	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR Ray Lasaki	6/26/85	TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD	
FINISH WAVETEK PROCESS	RELEASE APPROV Dean	6/26/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ±1° XX ± .030			
	DO NOT SCALE DWG		MODEL NO 23	DWG NO. 0103-00-1455 REV U
	SCALE		CODE IDENT 23338	SHEET 3 OF 6

0103-00-1455 U

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3294

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REV	ECN	BY	DATE	APP

FUNCTION SELECTOR

LF J7-13

SYNTH SIG (3A3)

TRI (2B1)

R165 2.49K
C84 .001
C88 .01
U30 1/4 DG211
C51 .1
R103 33.2K
R101 24.9K
R106 100K
R102 150
R100 500
SIN DIST D
SIN DIST B
R112 10K
CR67 FD777
CR71 FD777
CR69 FD777
CR68 FD777
CR70 FD777
R116 182
R113 200
SIN DIST A
CR66 FD777
R111 1K501K
R109 150
R105 500
SIN DIST C
R110 33.2K
R108 24.9K
C52 .1
SIN OFST
R107 100K
R114 221K
R104 46.4
C176 TRIM
R158 6.98K
Q27 2N5771
C87 .01
R164 2.49K
R163 4.99K
Q28 2N3906
CR34 1N4148
C83 .001
C86 .001
R156 10K
R162 4.99K
Q26 2N3906
R167 2.49K
R157 6.98K
Q25 2N5771
C85 .01
TRI OFST
R166 100K
R160 221K
R115 100
R161 200
R159 681
U30 1/4 DG211
C76 .1

PRE AMP

+15V
R128 2.49K
R127 2.49K
C68 .1
R132 7.5K
R131 1.5K
R130 2.49K
R129 2.49K
C144 .1
U30 1/4 DG211
CR33 1N4148
C72 .1
R149 33.2
Q29 2N3906
Q30 2N3906
R137 249
Q31 2N3640
C74 .1
R139 61.9
R155 100K
C82 .0033
Q37 5D215
FUNC OUT TO XY MULTI INPUT 5D8

PREAMP OFST
R147 100K
R145 301K
R148 1K
AD812
Q36
C78 100pF
R136 499
C70 .01
R133 10K
R134 499
R141 49.9
R140 10
Q33 2N3906
Q32 2N3563
C69 .01
C73 .1
R150 3.65K
R152 7.5K
R151 2.49K
R138 61.9
C79 .1
R144 2.49K
R146 10K
FUNCTST J15-6
SIN J7-14
TRI J7-15
SQR P5-7A

R143 2.49K
Q35 2N3904
R142 2K
Q34 2N3906
C75 .001

SQR SHAPER

TTLSQR (3B1)

R121 909 1/4W
R124 200
R120 1K
R119 1.5K 1/4W
Q24 2N3906
Q23 2N3904
CR31 2811
CR32 2811
R122 1.21K
R117 500
C53 .1
SQR TOP
R123 1.21K
R118 500
C71 .1
SQR BTM
E24
E25
E26
E27
C80 .0033
R153 100K
Q48 SD215
C81 *
R154 49.9

NOTE UNLESS OTHERWISE SPECIFIED
(SEE SHEET 1.)

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Jennifer Hatton	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR Kenji Sasaki	6/25/85	TITLE: SCHEMATIC, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV	6/26/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 23 · DWG NO. 0103-00-1455 · REV J
	SCALE		CODE IDENT 23338 · SHEET 4 OF 6

0103-00-1455 J

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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REV	ECN	BY	DATE	APP

XY MULTI AND P AMP

FUNC OUT (4C1)

VAMP J7-9

VNULL J7-8

VOFST J7-11

AMIN J20

PA OUT (6D1)

U31 MC1495L

U33 2540

U34 ½LF353

IT139 Q49

Q51 2N5160

Q52 2N2219A

Q53 2N3866

Q54 2N2905A

CR45 CR46 1N823(2)

CR48 1N4148

CR49 1N4148

CR50 1N5282

CR51 1N4148

CR52 1N5282

+15V

-15V

SIN AMPL

CY1

CY2

TRIM

NOTE. UNLESS OTHERWISE SPECIFIED
(SEE SHEET 1.)

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR 6/5/85		TITLE: SCHEMATIC, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV 6/26/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 23 / DWG NO 0103-00-1455 / REV J
	SCALE		CODE IDENT 23338 / SHEET 5 OF 6

0103-00-1455 J

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REV	ECN	BY	DATE	APP

1:1 LOCK LOOP

+5 L1 68µH C96 .1 C98 22/20 R181 1K

FSYNTH P14 E32 E33

HFSQ (3C1) E18 E19

U29 MC4044P

C97 22/20

+15 C106 10/25 R190 2.37K CR41 1N751A 5.1v

R189 1K C102 .1

R182 2K

Q42 2N4122 C105 .1 CR40 1N823

Q45 2N3904 C114 .1 CR42 1N4148 Q44 2N5485 C126 10pF

C100 10pF C101 .1 C99 10pF

U28 CA3049T

R194 1.5K C108 220pF R195 1.21K C112 .0047 R193 1.21K C107 .047 R192 1.21K C118 1/35 C117 1/35 C109 .01 MYLAR

C95 .01 C103 .1 C94 .1 R186 9.09K R185 9.09K

Q43 2N3904 C104 .1 R187 2.87K R184 500

PLL NULL

-15

+15 +5 C113 .047 C119 1/35 C122 22/20 C120 1/35 C121 68/15 C110 .1 C111 .1

U32 DG211

C125 .01 C123 .01 C116 .01 -15 C124 .1

R200 2.49K R197 2.49K R191 2.49K

CR43 1N823 R198 4.02K R201 4.99K R202 2K C135 22/20 -15

FR4 J7-4

FR5 J7-6

FR6 J7-5

ATTENUATOR

K1 RA30441051 K2 RA30441051

R259 4.99K R263 499 R260* R264 100 1W R261 10 R265 100 1W R262 10

Z OUT	
50Ω	JP1
75Ω	25Ω
600Ω	550Ω

PA OUT (5C1)

JP1 F3 FB 1/2 FUNC OUT J23

CR54 1N4002 CR56 1N4002 CR53 1N5349 CR55 1N5349

+5 Ā0 J7-16 C174 .001 C173 .001 Ā1 J7-17

V LOOP (1B8)

SYNC OUT DRIVERS

+5 FB1 C18 .1 C19 10/25 U15 ½S140

SYNC P9 E28 E29

E20 E21 E22 E23

+5 CR62 1N5282 CR63 1N5282 R10 182

+15 R208 470 ½W CR61 1N5282 F1 FB1/16 TTL OUT J21

C91 10/25

+15 R170 523 CR35 CR36 1N4148 (2) C93 .1 R171 523 Q39 2N3906 R168 499 R169 150

+5 R178 681 R172 2.49K

Q38 Q41 2N3640(2) Q40 2N3646

CR38 CR37 1N4148 (3) CR39 CR59 1N5282 CR60 1N5282 R173 1.21K F2 FB 1/16 J22 ECL OUT

R177 124 R174 750, ¼W R175 2.87K -15 C92 10/25

NOTE: UNLESS OTHERWISE SPECIFIED

(SEE SHEET 1.)

© BOWNE GRAPHICS & ACCUSPRESS RECORDER NO. A27888

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Dennis Batta	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	DSG. ENGR	6/4/85	TITLE: SCHEMATIC, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV	6/26/85	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		
	SCALE		MODEL NO 23 · DWG NO 0103-00-1455 · REV J · CODE IDENT 23338 · SHEET 6 OF 6

0103-00-1455

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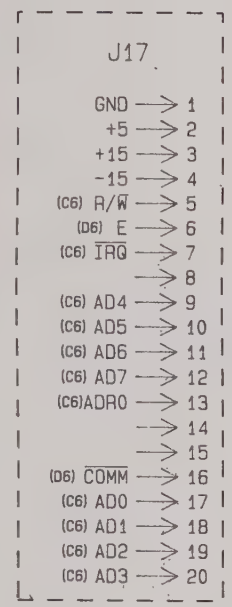
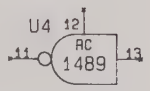
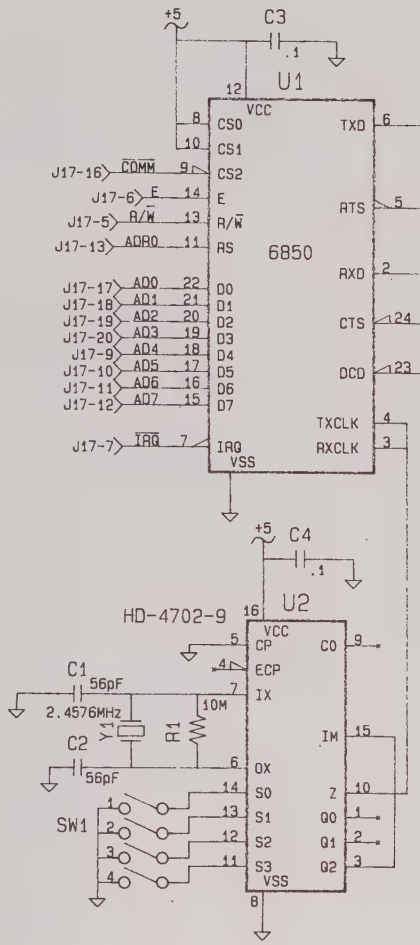
REV	ECN	BY	DATE	APP







4. CAPACITORS VALUED IN MICROFARADS (uF).
3. RESISTORS VALUED IN OHMS, 1/8W.
2. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN PREFIX WITH APPROPRIATE ASSEMBLY REFERENCE DESIGNATION. (SEE INSTRUMENT SCHEMATIC)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 7/5/95	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	3/24/95	TITLE: SCHEMATIC, RS-232 OPTION
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 23/75 · DWG NO 0103-00-1677 · REV A
	SCALE		CODE IDENT 23338 · SHEET OF

0103-00-1677 A

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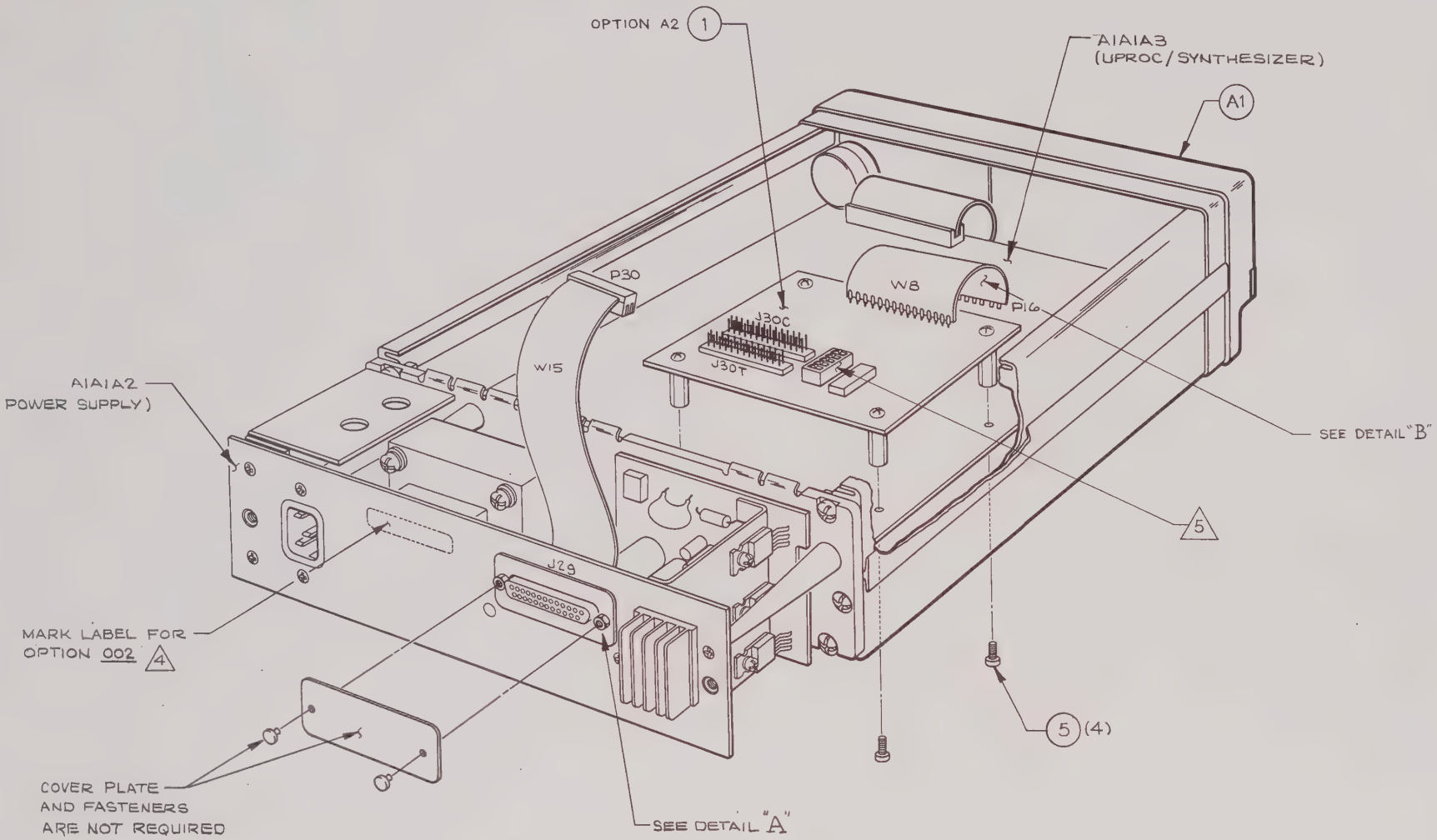
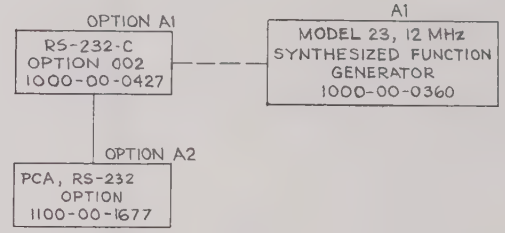
REV	ECN	BY	DATE	APP



INSTRUMENT COVERS NOT SHOWN

CABLE HOOKUP CHART		
REF DES	DESTINATION FROM	DESTINATION TO
W8	P16	A1A1A3-J16
W15	P30	OPTION A2-J30C 6



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, RS-232 OPTION	1100-00-1677	WVTK	1100-00-1677	1
2	PLATE, RS-232 ADAPTER	23/75-9643	WVTK	1400-01-9643	1
3	MODIFICATION, JACK SCREW: M/F: 2100-07-0021	23/75-9669	WVTK	1400-01-9669	2
4	LABEL, OPTION, MODEL 75	1400-01-9900	WVTK	1400-01-9900	1
5	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
W15	ASSY, RIBBON CABLE	6002-00-0029	WVTK	6002-00-0029	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 23/75 RS-232-C, OPTION 002	1000-00-0427	
		PAGE 1	

6. FACTORY CONFIGURED FOR DCE OPERATION. SEE INSTRUMENT INSTRUCTION MANUAL.
5. BAUD RATE SELECTOR SWITCH, FACTORY PRESET TO 9600 BAUD. SEE INSTRUMENT INSTRUCTION MANUAL.
4. IF OPTION INSTALLED ON MODEL 23, EXCEPT MODEL 23 SPECIAL, DO NOT USE LABEL 1400-01-9900.
3. INSTALL RS-232C CABLE/ALIGNMENT FIXTURE TO J29 WHILE TIGHTENING HARDWARE TO ENSURE CORRECT SPACING.
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 7/3/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE RS-232-C, OPTION 002
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 23/75	DWG NO 1000-00-0427 REV
	SCALE NONE	CODE IDENT 23338	

1000-00-0427

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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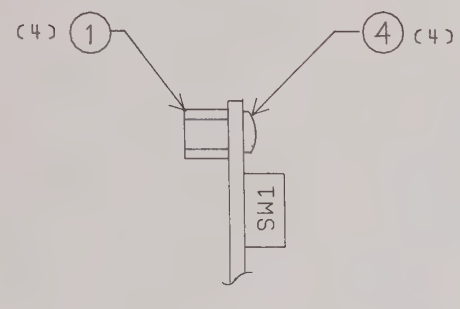
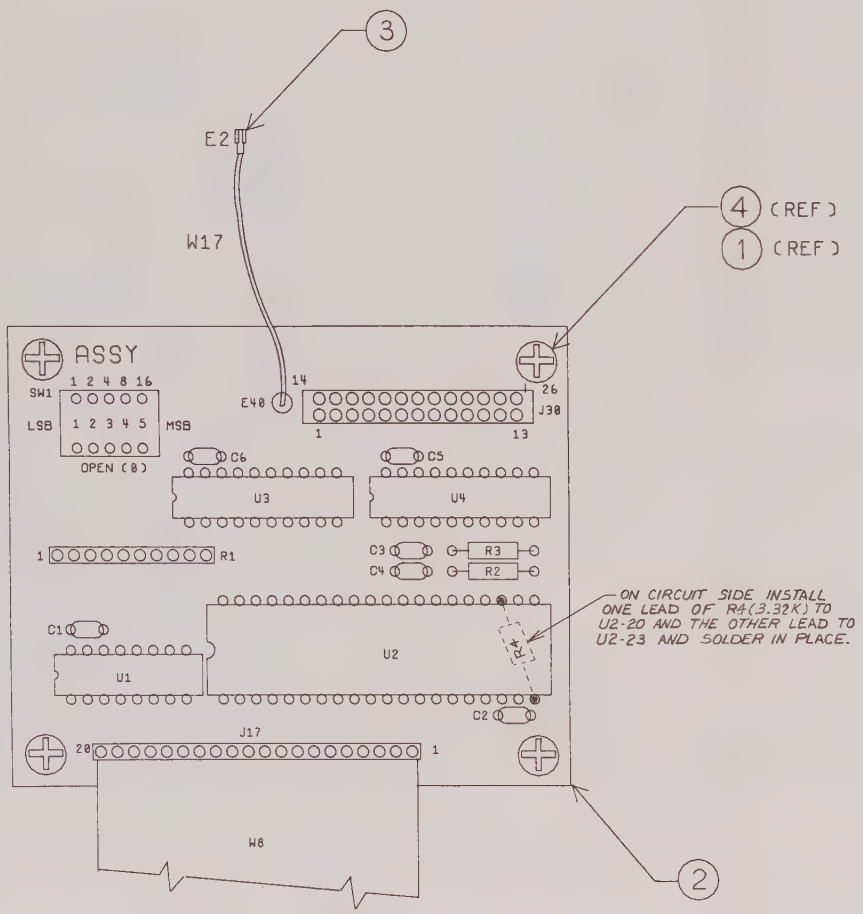
REV	ECN	BY	DATE	APP
A	ECO # 8129	M.C. 4-22-87	4-24-87	A.P.T.





CABLE HOOKUP CHART			
REF DES	AWG	LENGTH	COLOR
W17	18	[illegible]	GRN/YEL

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, GPIB OPTION	0103-00-1678	WVTK	0103-00-1678	1
1	STANDOFF	013-003-2	WVTK	1400-00-2503	4
C1 C2 C3 C4 C5 C6	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	6
2	GPIB OPTION BOARD	1700-00-1678	WVTK	1700-00-1678	1
J30	CONN, HEADER 26 PIN/2 ROW, .1 CTR, 15 GLD	929836-01-13	A/P	2100-02-0136	1
3	CONN, RECEPT, QUICK DISCONNECT	60358-1	AMP	2100-04-0044	1
4	SCREW, 4-40X3/16, PHP, NYLOK PATCH	4-40 X 3/16	CMRCL	2800-23-4103	4
R2 R3	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R4	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R1	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	1
SW1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
W17	WIRE, HU, 18GA	H0102003 (GRN/YEL)	JUDD	6000-31-8045	1
W8	CABLE FLEXIBLE FLAT 2" 20 PIN	1-88665-9	AMP	6001-60-0008	1
U2	ADPT, GPIB INTERFACE	MC68488P	MOT	8006-84-8800	1
U1	HEX BUS DRIVER	SN74HC368	TI	8007-43-6840	1
U3	XCVR, OSC BUS, TTL	75160	TI	8007-51-6000	1
U4	TRANSCEIVER, OCT BUS, TTL	SN75161BN	TI	8007-51-6100	1

4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.

3. SEE INSTRUMENT SCHEMATIC FOR ASSEMBLY INTERCONNECTION.

2. SEE 0103-00-1678 FOR CIRCUIT SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN B. REDMAN 5/3/85
PROJ ENGR M. STEINER 8/26/85
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE 2/1

WAVETEK SAN DIEGO • CALIFORNIA
TITLE PCA, GPIB OPTION
MODEL NO 23/75
DWG NO. 1100-00-1678
REV A
CODE IDENT 23338
SHEET 1 OF 1

BOOTH GRAPHICS ACCOUNT
REORDER NO. 837088

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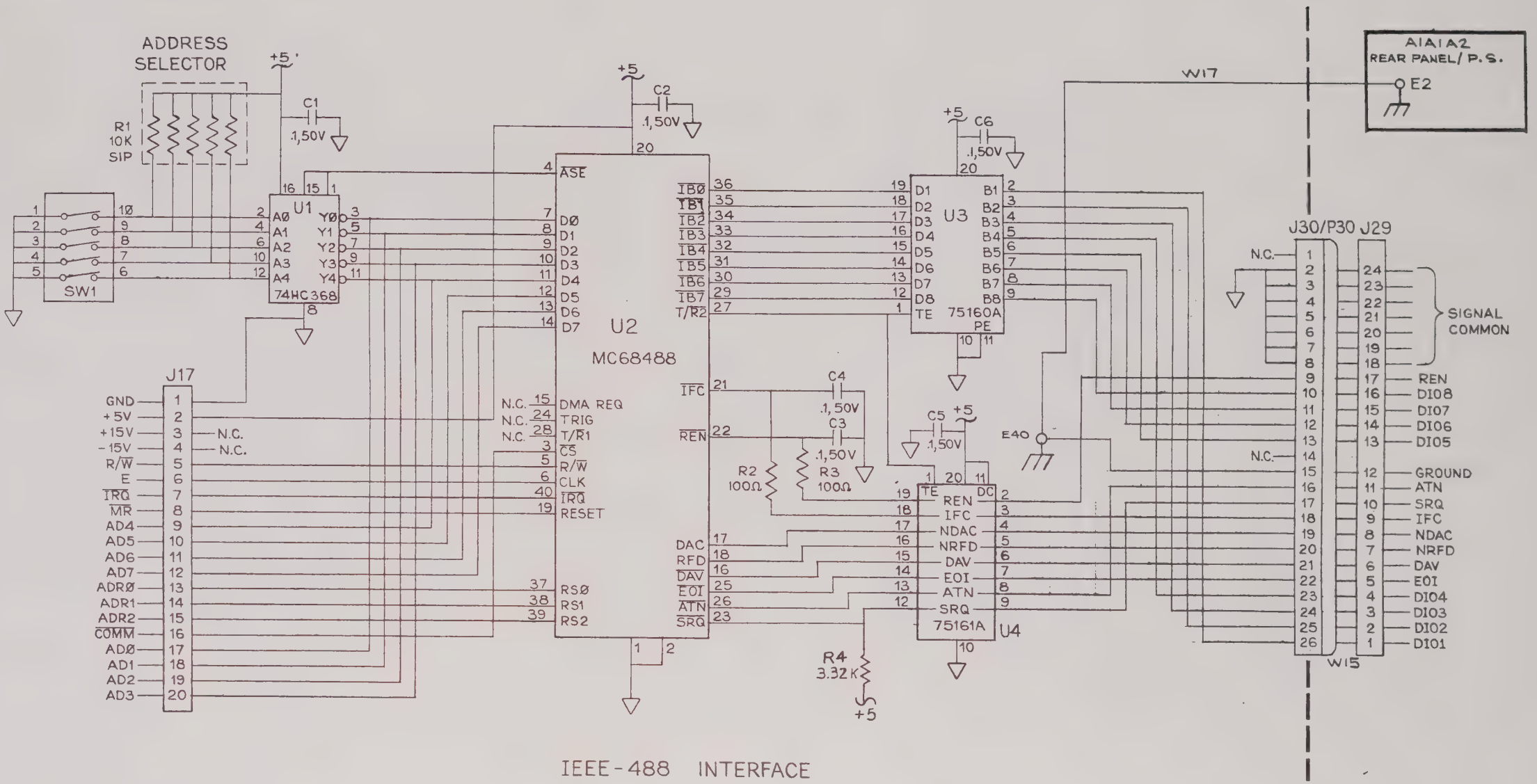
REV	ECO	BY	DATE	APPROVAL
A	ECO # 8129	J.C. 4-21-87	4-24-87	ART



IEEE-488 INTERFACE

2. CAPACITOR VALUES ARE IN MICROFARADS (μF).
1. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 3/1/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR H. STEINER	8/26/85	TITLE SCHEMATIC, GPIB OPTION
FINISH WAVETEK PROCESS —	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 23/75 · DWG NO. 0103-00-1678 · REV A
	SCALE —		CODE IDENT 23338 · SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-4831

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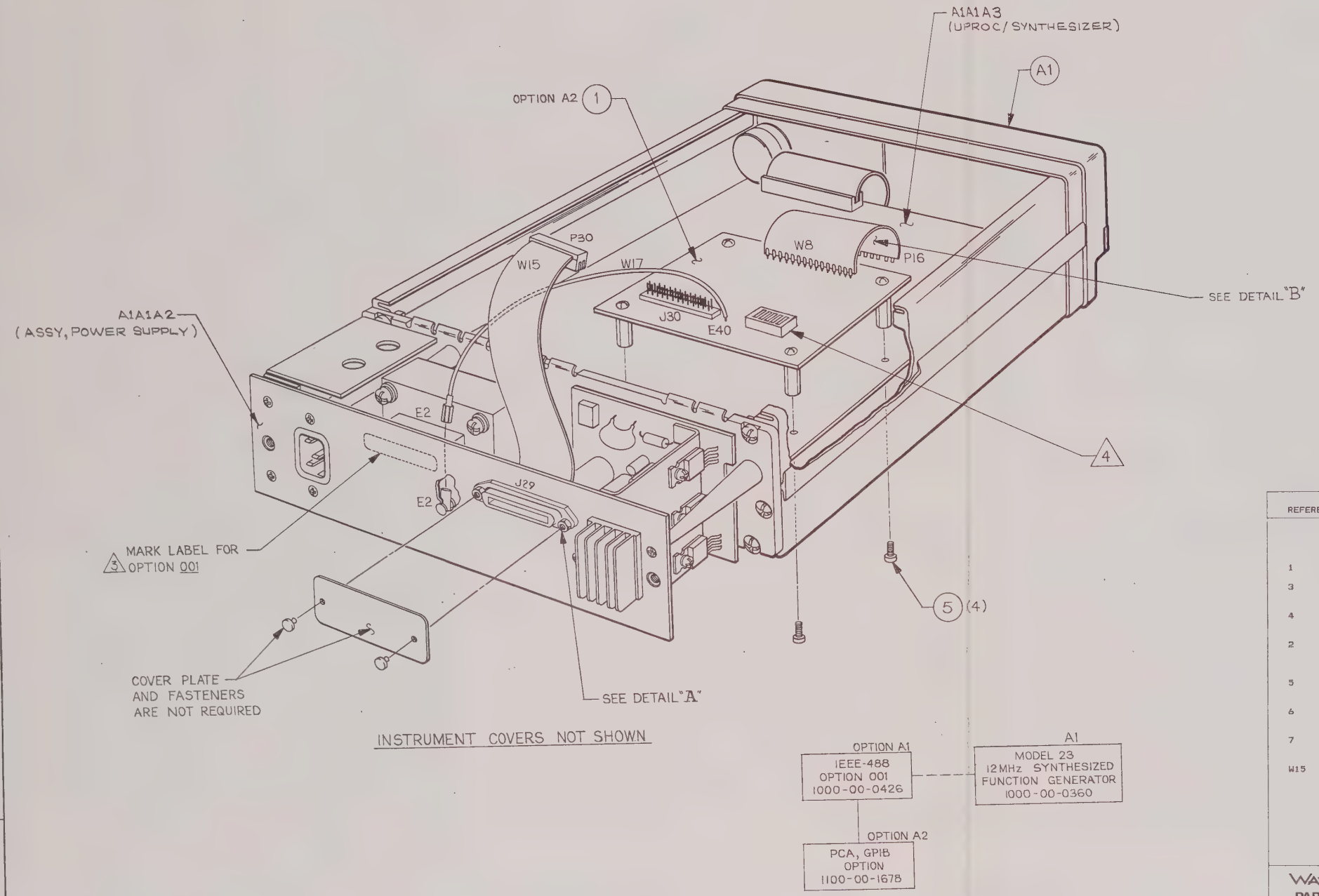
REV	ECN	BY	DATE
A	ECO # 8120	[illegible] 9/18-81	7/-82



INSTRUMENT COVERS NOT SHOWN

CABLE HOOKUP CHART		
REF DES	DESTINATION FROM	TO
W8	P16	A1A1A3-J16
W15	P30	OPTION A1-J30
W17	E2	A1A1A2-E2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, GPIB OPTION	1100-00-1678	WVTK	1100-00-1678	1
3	LABEL, OPTION, MODEL 75	1400-01-9900	WVTK	1400-01-9900	1
4	NUT, HEX, CAD PLATE 6-32	MS35649-264	COML	2800-14-6100	2
2	SCREW, JACK, 3.5MMX.6MM THD, F, 6-32 M THD, .85LG	2800-23-0033	POSIT	2800-23-0033	2
5	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
6	WASHER, FLAT, #6 BIN 495	#6FLAT WASHER	CMRCL	2800-26-6001	2
7	WASHER, SPLIT LOCK #6 6	#6SRLW	CMRCL	2800-42-6000	2
W15	ASSY, GPIB RIBBON CABLE	6002-00-0030	WVTK	6002-00-0030	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 23/75 IEEE-488, OPTION 001	1000-00-0426	A
		PAGE 1	

4. ADDRESS SELECTOR SWITCH, FACTORY PRESET TO 9. SEE INSTRUMENT INSTRUCTION MANUAL.

3. IF INSTALLED ON MODEL 23, EXCEPT MODEL 23 SPECIAL, DO NOT USE LABEL 1400-01-9900.

2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 7/5/85	WAVETEK SAN DIEGO, CALIFO
MATERIAL —	PROJ ENGR [illegible]		TITLE IEEE-488 OPTION 001
FINISH WAVETEK PROCESS —	RELEASE APPROV [illegible]		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 23/75	DWG NO 1000-00-0426 REV A
	SCALE NONE	CODE IDENT 23338	

BISHOP GRAPHICS ACCUPRESS

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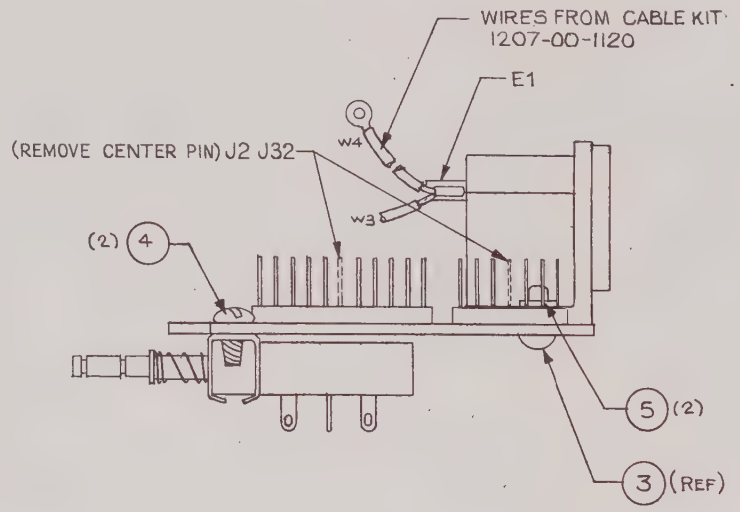
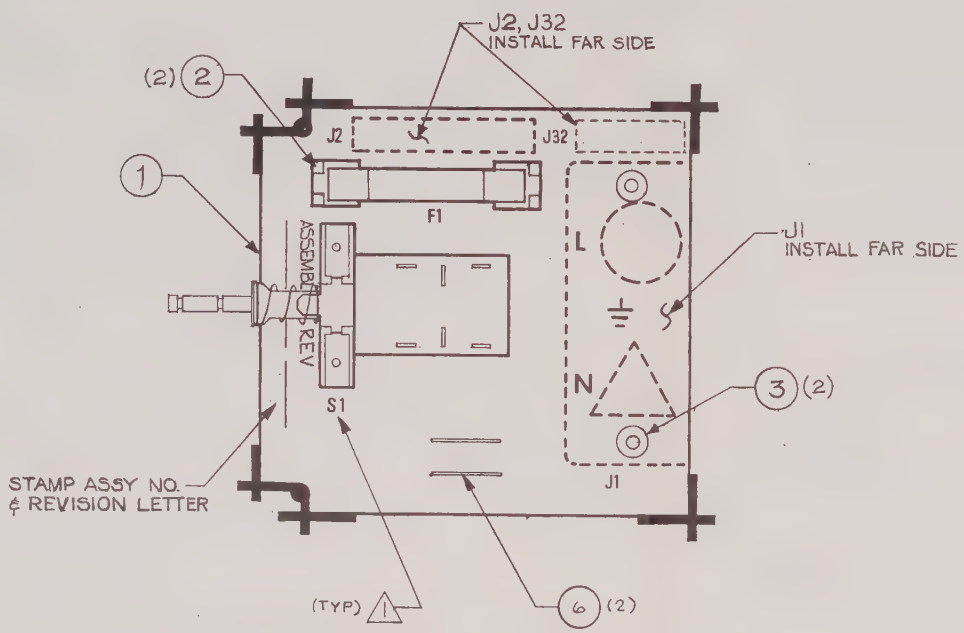
REV	ECN	BY	DATE	APP
A	#425145464250	KA	11/4/85	A.E.T.
B	#4595	DT	4/25/85	A.E.T.





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	AC PRIMARY BD	21-1119	WVTK	1700-00-1119	1
J2	CONN, HEADER, 11 PIN	1-87224-1	AMP	2100-02-0144	1
J32	CONN, HEADER, UNSHROUDED, 7 PIN	87224-7	AMP	2100-02-0184	1
J1	CONN, RECEPT, POWER (PC)	EAC-303	SWCFT	2100-03-0069	1
2	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	2
3	RIVET, ALUM 5/16X1/8 DIA .188-250	1125-0410	AVDEL	2800-12-0047	2
4	SCREW, 4X1/4 PHP SMS TYPE B	4-24 X 1/4	CMRCL	2800-22-4142	2
5	FLAT WASHER #4, .312 O.D., AN9604	#4FW	CMRCL	2800-26-4000	2
6	RES, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	2
S1	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST | TITLE: PCA, AC PRIMARY | ASSEMBLY NO. 1208-00-1119 | REV B | PAGE 1

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A2.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL — | FINISH WAVETEK PROCESS —

DRAWN A. TALMADGE 5/19/83 | PROJ ENGR 10/4/83 | RELEASE APPROV 11/4/83 | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX .030 | DO NOT SCALE DWG | SCALE 2/1

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PCA, AC PRIMARY (A2A2)

MODEL NO 21/22 | DWG NO 1208-00-1119 | REV B | CODE IDENT 23338 | SHEET | OF

1208-00-1119 B

ESHOP GRAPHICS/ACCUPRESS REORDER NO. A3994

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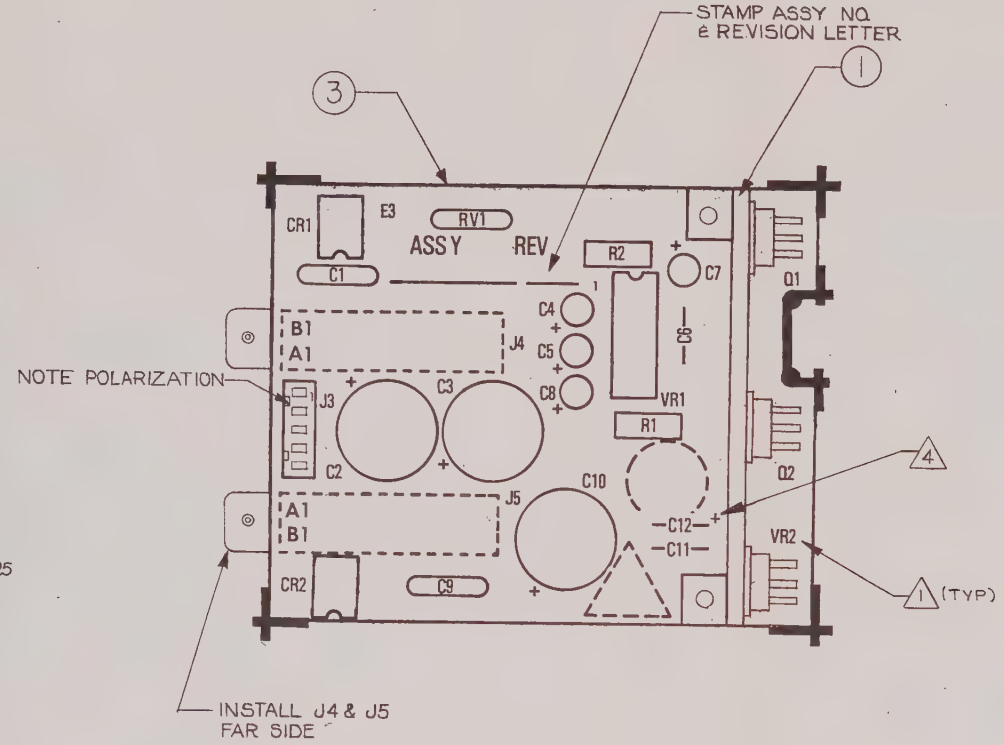
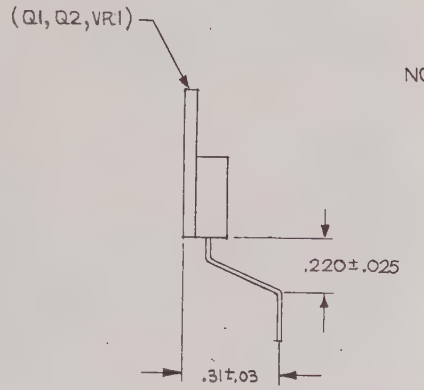
REV	ECN	BY	DATE	APP
A	#4667	MF	9/22/85	A.R.T.
B	#4728	KA	11/10/85	A.R.T.
C	#4999			
D	#7577	AT	7/11/86	A.R.T.
E	#7652	AT	9/24/86	A.R.T.
F	#7784	DT	11/21/86	A.R.T.

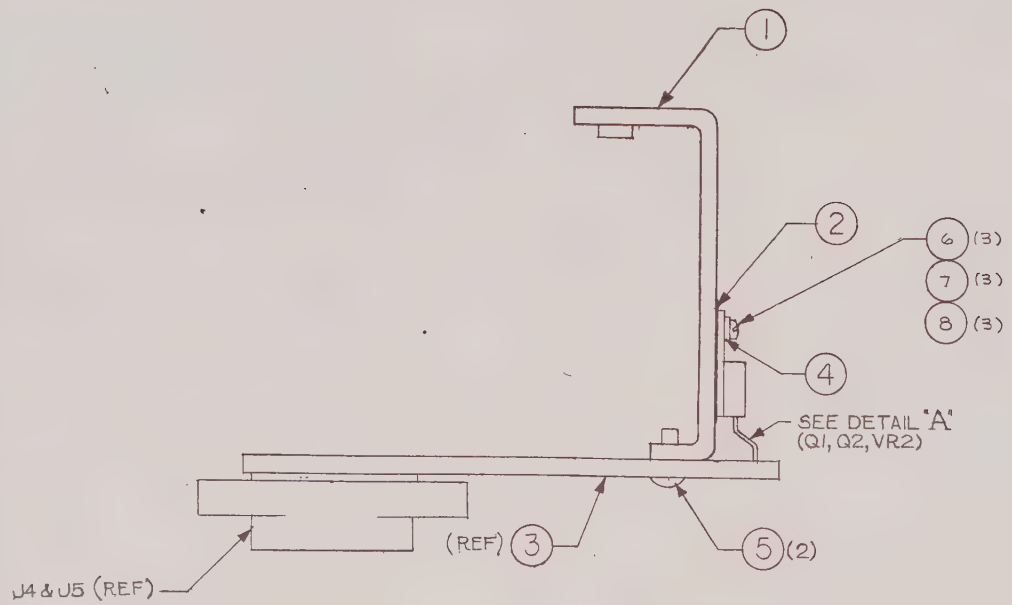




DETAIL A
(SCALE: NONE)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	BRKT, HEATSINK	21-8173	WVTK	1400-01-8173	1
C1 C9	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	2
C11 C6	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	2
C12 C7 C8	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	NRE 10/63	NIC	1500-31-0002	3
C2 C3	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	NRE 1000/50	NIC	1500-31-0203	2
C10	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	NRE 2200/16	NIC	1500-32-2201	1
C4 C5	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	ULB1H4R7M	NICH	1500-34-7903	2
3	POWER SUPPLY BD	21-1118	WVTK	1700-00-1118	1
J4 J5	CONN (20 PIN)	ETCIODRTI	SULIN	2100-02-0139	2
J3	CONN, HEADER 5 PIN	102202-2	AMP	2100-02-0143	1
4	WASHER	B51547F015	MOT	2800-11-0015	3
5	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
6	SCREW, 4X3/8 PHP SMS	4-24 X 3/8	CMRCL	2800-22-4162	3

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1208-00-1118 | REV F | PAGE 1



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	TYPE B				
7	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	3
8	#4 LOCKWASHER, PLATED	#4SRLW	CMRCL	2800-42-4000	3
2	INSULATOR (TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	3
RV1	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
R1 R2	RES, MF, 1/2W, 5%, .51 OHM	CMF60-0R51JT-00	DALE	4799-00-0144	2
CR1	DIODE, ZENER, 100V, 10% TOL, 1W, IN4764	VM18	VARO	4801-02-0008	1
CR2	DIODE, RECTIFIER, DUAL IN-LINE	VSB54	VARO	4806-02-0054	1
Q1 Q2	TRANS, NPN, TO-220	TIP-29	TI	4902-00-0290	2
VR1	VOLT REGULATOR	LM325AN	NSC	7000-03-2501	1
VR2	VOLT REGULATOR	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1208-00-1118 | REV F | PAGE 2

4. INSTALL C12 OBSERVING INDICATED POLARITY.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A1.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE 6/3/85	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL —	PROJ ENGR 10-17-85	TITLE	
	RELEASE APPROV 11/4/85	PCA, POWER SUPPLY (A 2A1)	
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 1208-00-1118 REV F
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 1

1208-00-1118 F

B-SHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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REV	ECN	BY	DATE	APP
B	# 4668, 4707	A.T.	3/4/85	A.R.T.
C	#4728	KA	9/10/85	A.R.T.
D	#6028	[illegible]	2/1/86	A.R.T.
E	#7577	A.T.	7/11/86	A.R.T.
F	#7695	AT	9/15/86	A.R.T.
G	#7784	AT	11/20/86	A.R.T.

A2 A2
PCA AC PRIMARY
1208-00-1119

F1		
MODEL	115	230
21/22	3/8 A	3/16A
23	1/2 A	1/4 A
75	3/8 A	3/16A

NOTE FOR 230V HOOK-UP INVERT CONNECTOR P2 AS SHOWN BELOW

J2-	P2-
1	11
2	10
3	9
4	8
5	7
6	6
7	5
8	4
9	3
10	2
11	1

A2 A1
PCA POWER SUPPLY
1208-00-1118 (MODEL 21/22/23)
1208-00-1772 (MODEL 75)

J32 1 2 3 4 5 6 7

OFF ON S1 — 4 F1 — (115V HOOK-UP) J2- P2-

J1: HOT, NEUT, GND — E1 — GRN/YEL (W4) — E2

(W3) GRN/YEL — E3

A2 T1

BLK	RED
N.C.	WHT/RED
WHT/BLK	RED
N.C.	
GRY	BLU
N.C.	
WHT/GRY	BLU
N.C.	

P3- J3-: 4, 3, 5, 1, 2

CR1 VM18 — C1 .01 GAP — C9 .01 GAP — CR2 VSB54

C2 1000/50V — C3 1000/50V — C4 4.7/50V — C5 4.7/50V

VR1 LM325A OR LM125 — Q1 TIP29 — Q2 TIP29 — R1 3 — R2 3

C6 .1/50V — C7 10/25V — C8 10/25V

+15V — -15V

VR2 LM7805 (IN, OUT, COM) — +5V

C10 2200/16V — C11 .1 — C12 10/25V

RV1 V56ZA8

J4- A1 B1 … A10 B10 — -15V, +5V, +15V

J5- A1 B1 … A10 B10

J31 1 2 3 4 5 6

P32 1 2 3 4 5 6 7 — P2 1 2 3 4 5 6 7 8 9 10 11

BLK	RED (P3 2)
ORN	WHT/RED (P3 3)
WHT/BLK	RED (P3 1)
GRY	BLU (P3 5)
VIO	
WHT/GRY	BLU (P3 4)

CONNECTIONS FOR TRANSFORMER WITH HI/LO AND 115/230V PRIMARIES

(SHOWN IN 115V, HI POSITION – REVERSE P32 FOR LO POSITION)

4 FOR FUSE P/N SEE:
MODEL 21/22-1101-00-1113
MODEL 23-1101-00-1703
MODEL 75-1101-00-1771

3 R1 AND R2 VALUES:
0.51Ω, 1/2 W (MODEL 21/22/23)
1.5Ω 1/2 W (MODEL 75)

2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2.

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 5.13.82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR [illegible]	10/14/82	TITLE: SCHEMATIC, POWER SUPPLY (A2)
FINISH WAVETEK PROCESS —	RELEASE APPROV [illegible]	11/4/83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		
	SCALE —		

MODEL NO	DWG NO	REV
21/22	0103-00-1113	G
CODE IDENT 23338	SHEET 1 OF 1	

0103-00-1113 G

B/SHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U31	IC	MC1495L	MOT	7000-14-9500	1
U33	IC, LIN, OP-AMP, WIDE BAND	HA1-2540-5	HARIS	7000-25-4000	1
U22	IC	CA-3019	RCA	7000-30-1900	1
U28	IC	CA3049T	RCA	7000-30-4900	1
U25	IC	CA-3096AE	RCA	7000-30-9600	1
U26 U30 U32	CMOS, SW, QUAD ANALOG	DG211CJ	SILX	8000-02-1100	3
U2	GATE, NAND, QUAD 2INP, TTL	74F00PC	FAIR	8000-74-0002	1
U16 U8 U9	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	3
U12	GATE, NOR, QUAD, 2INP, TTL	74LS02	TI	8000-74-0210	1
U1 U19	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	2
U18	GATE AND, QUAD 2-INP, TTL	74LS08	TI	8000-74-0810	1
U5	GATE AND, 3-INP, TTL	74F11PC	FAIR	8000-74-1102	1
U10 U3	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, WAVEFORM GEN BD	1100-00-1455	J
		PAGE 13	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U11	TTL, XOR, QUAD 2INP	74LS86	TI	8000-74-8610	1
U4	TTL, F/F, DUAL J-K	74LS107A	TI	8007-41-0710	1
U20	TTL, NAND, 13INP	74LS133	FAIR	8007-41-3310	1
U15	IC	74S140	TI	8007-41-4001	1
U13 U6	COUNTER, SYNC 4 UP-DN, TTL	SN74LS169BN	TI	8007-41-6911	2
U14	TTL, D-F/F, OCT	74LS374	TI	8007-43-7410	1
U17	COUNTER, DUAL 4B BCD, CMOS	MM74HC390N	NSC	8007-43-9040	1
U29	IC	MC4044P	MOT	8100-40-4400	1
U7	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0249	WVTK	8600-00-0249	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, WAVEFORM GEN BD	1100-00-1455	J
		PAGE 14	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST WAVEFORM GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 23 / DWG NO 1100-00-1455 / QTY J
	SCALE		CODE IDENT 23338 / SHEET 3 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFOR MATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R143 R144 R15 R151 R16 R164 R165 R167 R172 R191 R197 R200 R35 R60 R62 R63 R65 R76 R80 R81 R89 R90 R91 R93					
R101 R108 R226	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	3
R237	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R175 R187	RES, MF, 1/8W, 1%, 2.87K	RN55D-2871F	TRW	4701-03-2871	2
R243	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R190 R30	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	2
R145	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R38 R42 R48 R52	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	4
R103 R110	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R149 R53 R55	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R224	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R218 R87	RES, MF, 1/8W, 1%, 35.7K	RN55D-3572F	TRW	4701-03-3572	2
R150	RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R238T	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R198 R215	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	2

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R211 R67	RES, MF, 1/8W, 1%, 40.2K	RN55D-4022F	TRW	4701-03-4022	2
R25	RES, MF, 1/8W, 1%, 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R31	RES, MF, 1/8W, 1%, 4.32K	RN55D-4321F	TRW	4701-03-4321	1
R57	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	1
R104 R242 R255	RES, MF, 1.8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	3
R126	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	1
R134 R136 R168 R220 R221 R263	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	6
R162 R163 R201 R216 R217 R239 R259 R78 R83 R84 R97	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	11
R141 R154 R207 R236	RES, MF, 1/8W, 1%, 49.9	RN55D-49R9F	CORNO	4701-03-4999	4
R260T	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R170 R171 R234 R235	RES, MF, 1/8W, 1%, 523	RN55D-5230F	TRW	4701-03-5230	4
R210	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	1
R222	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	1
R39	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R138 R139	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	2
R159 R178 R229	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	3

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R3	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R13 R157 R158 R21	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	4
R244T R256T	RES, MF, 1/8W, 1%, 69.8	RN55D-69R8F	TRW	4701-03-6989	2
R206	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R132 R152 R4 R8	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	4
R82	RES, MF, 1/8W, 1%, 75K	RN55D-7502F	CORNO	4701-03-7502	1
R85	RES, MF, 1/8W, 1%, 8.06K	RN55D-8061F	TRW	4701-03-8061	1
R98	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R185 R186	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	2
R95	RES, MF, 1/8W, 1%, 90.9K	RN55D-9092F	TRW	4701-03-9092	1
R11 R17 R20	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	3
R209	RES, MF, 1/8W, 1%, 9.53K	RN55D-9531F	TRW	4701-03-9531	1
R94	RES, MF, 1/8W, 1%, 9.76K	RN55D-9761F	TRW	4701-03-9761	1
R231	RES, MF, 1/4W, 1%, 121	RN60D-1210F	TRW	4701-13-1210	1
R119	RES, MF, 1/4W, 1%, 1.5K	RN60D1501F	TRW	4701-13-1501	1
R40	RES, MF, 1/4W, 1%, 499	RN60D4990F	TRW	4701-13-4990	1

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R174	RES, MF, 1/4W, 1%, 750	RN60D7500F	TRW	4701-13-7500	1
R121	RES, MF, 1/4W, 1%, 909	RN60D9090F	TRW	4701-13-9090	1
R264 R265	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
U27	RES MODULE	4116R-001-102	BOURN	4770-00-0019	1
R5 R6 R7	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	3
JP1 R22	RESISTOR, 0 OHM JUMPER	JP02T6B0	RCHM	4799-00-0087	2
CR41	DIODE	1N751A	FAIR	4801-01-0751	1
CR40 CR43 CR45 CR46	DIODE, ZENER 6.2V	1NB23A	MOT	4801-01-0823	4
CR24 CR25	DIODE	1N959	SIEM	4801-01-0959	2
CR15 CR22	DIODE	1N4740A	MOT	4801-01-4740	2
CR3 CR4 CR5 CR50 CR52 CR59 CR6 CR60 CR61 CR62 CR63 CR7 CR8	DIODE	1N5282	FAIR	4801-01-5282	13
CR53 CR55	DIODE	1N5349A	MOT	4801-01-5349	2
CR54 CR56	DIODE, IN4002 GEN. PURPOSE, RECT. 100V, 1A	1N4002	FAIR	4801-02-0001	2
CR10 CR11 CR12 CR13 CR14 CR57 CR58	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	7

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
CR1 CR16 CR17 CR2 CR20 CR21 CR23 CR26 CR27 CR28 CR29 CR30 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR42 CR44 CR48 CR49 CR51 CR72 CR73 CR74 CR75 CR9	DIODE	1N4148	FAIR	4807-02-6666	29
CR18 CR19 CR31 CR32 CR64 CR65	DIODE	5082-2811	HP	4809-02-2811	6
CR66 CR67 CR68 CR69 CR70 CR71	DIODE, SET, 6-FD-777, QTY: 6: 4807-02-0777	4898-00-0021	WVTK	4898-00-0021	1
Q52	TRANS	2N2219A	NSC	4901-02-2191	1
Q54	TRANS	2N2905A	NSC	4901-02-9051	1
Q11 Q16 Q32	TRANS	2N3563	FAIR	4901-03-5630	3
Q31 Q38 Q41	TRANS, PNP, TO-92	2N3640	FAIR	4901-03-6400	3
Q40	TRANS	2N3646	NSC	4901-03-6460	1
Q53	TRANS	2N3866	MOT	4901-03-8660	1
Q18 Q20 Q21 Q23 Q35 Q43 Q45 Q8	TRANS	2N3904	FAIR	4901-03-9040	8
Q1 Q19 Q2 Q24 Q26 Q28 Q29 Q3 Q30 Q33 Q34 Q39 Q9	TRANS	2N3906	FAIR	4901-03-9060	13
Q42	TRANS, GENERAL PURPOSE, PNP, TO-92	2N4122	NSC	4901-04-1220	1

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q51	TRANS	2N5160-18	MOT	4901-05-1600	1
Q5	TRANS	2N5462	MOT	4901-05-4620	1
Q4 Q44	TRANS	2N5485	MOT	4901-05-4850	2
Q10 Q14 Q15 Q17 Q25 Q27	TRANS	2N5771	NSC	4901-05-7710	6
Q49	TRANS	IT 139	INTSL	4902-00-1390	1
Q37 Q48	TRANS	SD214DE/BR	SIQ	4902-00-2140	2
Q12	TRANS, M/PR, 2N3563 QTY: 2: 4901-03-5630	142-501-52	WVTK	4998-00-0004	1
Q6 Q7	TRANS, M/PR, 2N5485 QTY: 2: 4901-05-4850	142-501-53	WVTK	4998-00-0009	1
R111	THERMISTER	1K-501-K	MCI	5300-00-0011	1
R253 R61	THERMISTER	1K-101-K	MCI	5300-00-0012	2
W1	CABLE, FLEXIBLE FLAT, 7", 20PIN	1-88667-9	AMP	6001-60-0006	1
U21	IC	DAC-08EQ	AMD	7000-00-0800	1
U23	IC	TL084CN	TI	7000-00-8400	1
U34	IC	LF353N	NSC	7000-03-5300	1
Q36	IC	AD 812	ANDEV	7000-08-1200	1

WAVETEK PARTS LIST | TITLE PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
WAVEFORM GENERATOR BD

SIZE	DWG NO	REV
D	1100-00-1455	J
CODE IDENT 23338	SHEET 2 OF 3	

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC WAVEFORM GEN BD	0103-00-1455	WVTK	0103-00-1455	1
C49	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	1
C100 C126 C99	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	3
C17 C54 C56 C78	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	4
C173 C174 C32 C33 C34 C75 C83 C84 C86	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	9
C116 C123 C125 C15 C61 C62 C63 C64 C69 C70 C85 C87 C88 C95	CAP, CER, MN, .01MF, 50V Z5U, +80/-20% RAD LEAD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	14
C1 C10 C101 C102 C103 C104 C105 C11 C110 C111 C114 C12 C124 C127 C128 C13 C130 C132 C136 C137 C138 C139 C14 C142 C143 C144 C151 C157 C158 C16 C161 C162 C163 C164 C169 C175 C18 C2 C23 C30 C31 C35 C36 C39 C4 C40 C41 C42 C43 C44 C45 C47 C48 C5 C50 C51 C52 C53 C55 C57 C58 C59 C6 C60 C65 C68 C7 C71 C72 C73 C74 C76 C79 C8 C89 C9 C93 C94 C96	CAP, CER, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	79
C24T	CAP, CER, .0015MF, 1KV	DD-152 LONG LEAD	CRL	1500-01-5201	1
C146T C154 C156T	CAP, CER, 1.5PF, 1KV	NCD1.5PF1KVK750-CR	NIC	1500-01-5507	3

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C109	CAP, MYLAR, .01MF, 100V	225P10391WD3	SPRAG	1500-41-0314	1
C112	CAP, MLAR, .0047MF100V	225P47291WD3	SPRAG	1500-44-7204	1
C107 C113	CAP, MYLAR, .047MF100V	225P47391WD3	SPRAG	1500-44-7314	2
C37	VARI, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	1
C153	CAP, VAR, 3-18PF	GKU18000	SPRAG	1500-51-8010	1
C38	VARI, 7-35PF, 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-3000	1
C117 C118 C119 C120	CAP, TANT, 1MF, 35V	196D105X0035HA1	SPRAG	1500-71-0512	4
C122 C133 C134 C135 C140 C141 C159 C160 C171 C172 C97 C98	CAP, TANT, 22MF, 20V	202A2002226M3	MATSO	1500-72-2621	12
C131	CAP, TANT, 33MF, 6V	196D336X0006JE3	SPRAG	1500-73-3600	1
C121 C66	CAP, TANT, 6.8MF, 50V	TAPB6.8M50	ITT	1500-76-8503	2
C27 C28	CAP, SET POLY MIXED MATCH SET	1509-80-0012	WVTK	1509-80-0012	1
1	DRILL DRWG, WAVEFORM GEN BD	1700-00-1455	WVTK	1700-00-1455	1
L1	CHOKE, 68 MICRO HENRY	IR-2	DALE	1800-00-0018	1
J18 J19 J20 J21 J22 J23	CONNECTOR, BNC(PC)	227161-1	AMP	2100-01-0019	6

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R203 R214 R66	POT, TRIM, 20K	91AR20K	BECK	4600-02-0301	3
R100 R105 R117 R118 R125 R184 R2 R223 R251	POT, TRIM, 500	91AR500	BECK	4600-05-0104	9
R32 R33 R34 R44 R45	RES, C, 1/2W, 5%, 4.7	RC-1/2-4R7J	STKPL	4700-25-0479	5
R24	RES, C, 1/2W, 5%, 1K	RC-1/2-102J	STKPL	4700-25-1001	1
R208	RES, C, 1/2W, 5%, 470	RC20GF-471	STKPL	4700-25-4700	1
R115 R23 R37 R47 R49 R50 R58	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	7
R120 R148 R181 R189 R227 R250 R68 R71 R74	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	9
R112 R133 R146 R156 R212 R51 R79 R92 R99	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	9
R153 R155	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	2
R69 R72 R77	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	3
R140 R240 R241 R245 R248 R249 R261 R262 R36 R46	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	10
R29	RES, MF, 1/8W, 1%, 10.5K	RN55D-1052F	TRW	4701-03-1052	1
R233 R28	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	2
R122 R123 R173 R192 R193 R195 R213	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	7

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C167 C168T	CAP, CER, 22PF, 1KV	DD-220 LONG LEAD	CRL	1500-02-2001	2
C67	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C148 C90	CAP, CER, .0022, 1KV	DD-222SLL	CRL	1500-02-2201	2
C80 C82	CAP, C, MN, 3300PF, 50V	1801X7R050A332J	VRDYN	1500-03-3205	2
C155T	CAP, CER, 47PF, 1KV	DD-470 LONG LEAD	CRL	1500-04-7001	1
C81T	CAP, CER, 56PF, 1KV	DD-560	CRL	1500-05-6001	1
C145 C165	CAP, CER, 820PF, 1KV	DD-821 LONG LEAD	CRL	1500-08-2101	2
C108	CAP, MICA, 220PF, 500V	DM15-221J	ARCO	1500-12-2100	1
C46	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	1
C23T	CAP, MICA, 36PF, 500V	DM15-360J	ARCO	1500-13-6000	1
C26T	CAP, MICA, 75PF, 500V	DM15-750J	ARCO	1500-17-5000	1
C29	CAP, MICA, 820PF, 300V	DM15-821F	ARCO	1500-18-2101	1
C106 C19 C91 C92	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	4
C21 C22	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	2
C20	CAP, ELECT, 100MF/16V RADIAL LEAD, SP .20	CRE SERIES 100/16	CAPAR	1500-31-0111	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
XU11 XU33	SKT, IC, 14 PIN	DIL814P-10BT	BURND	2100-03-0066	2
2	SOCKET, MINISERT	75060-012	BERG	2100-03-0076	12
J15	HEADER, 14 PIN, 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
F3	FUSE, 1/2A, 125V(PC)	255.500	LITFU	2400-05-0035	1
F1 F2	FUSE, AXILAL LD 1/16A	255.062	LITFU	2400-05-0040	2
3	HEAT SINK	207	WAKE	2800-11-0001	2
4	TRANSIPAD	10123N	METRS	2800-11-0003	1
5	TRANSIPAD	333-125-NY	BLINN	2800-11-0017	3
FB1	FERRITE BEAD	56-390-65/3B	FERRX	3100-00-0001	1
K1 K2	RELAY, FORM C, DIP	RA30441051-02	ETROL	4500-00-0018	2
R26	POT, TRIM, 100	91AR100	BECK	4600-01-0103	1
R204	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	1
R106 R107 R147 R166 R247 R70 R73 R88 R96	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	9
R232 R258	POT, TRIM, 20	91AR20	BECK	4600-02-0000	2
R113 R161	POT, TRIM, 200	91AR200	BECK	4600-02-0101	2
R86	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R177	RES, MF, 1/8W, 1%, 124	RN55D-1240F	TRW	4701-03-1240	1
R179	RES, MF, 1/8W, 1%, 13.7K	RN55D-1372F	TRW	4701-03-1372	1
R102 R109 R169	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	3
R131 R194 R43	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	3
R1	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R12	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R230 R41	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R10 R116	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	2
R124	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R142 R182 R183 R202 R219 R54 R56 R75	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	8
R18 R19 R9	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R225 R228	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R114 R160	RES, MF, 1/8W, 1%, 221K	RN55D-2213F	TRW	4701-03-2213	2
R190 R246 R252 R59	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	4
R137 R205	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R127 R128 R129 R130 R14	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	29

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN BD | ASSEMBLY NO. 1100-00-1455 | REV J | PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST WAVEFORM GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 23 / DWG NO 1100-00-1455 / REV J
	SCALE		CODE IDENT 23338 / SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A2788

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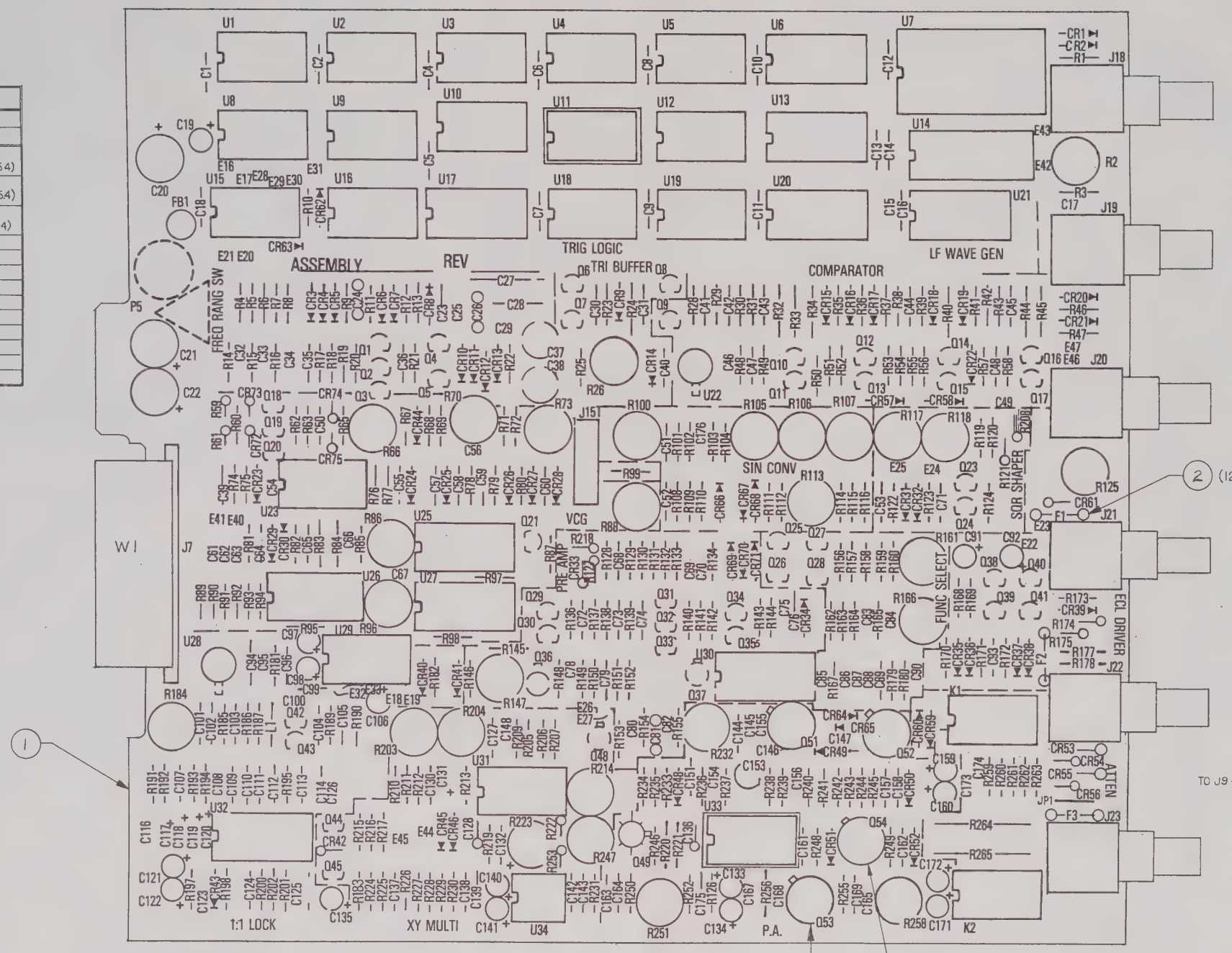
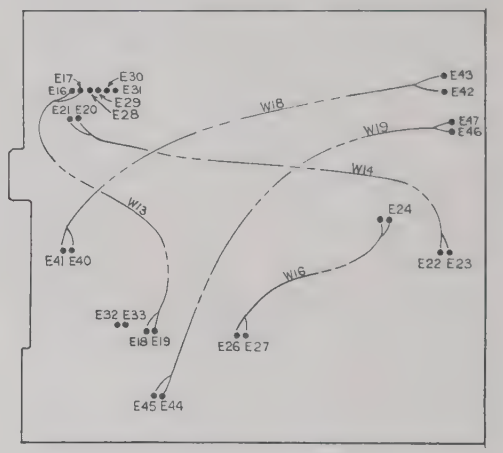
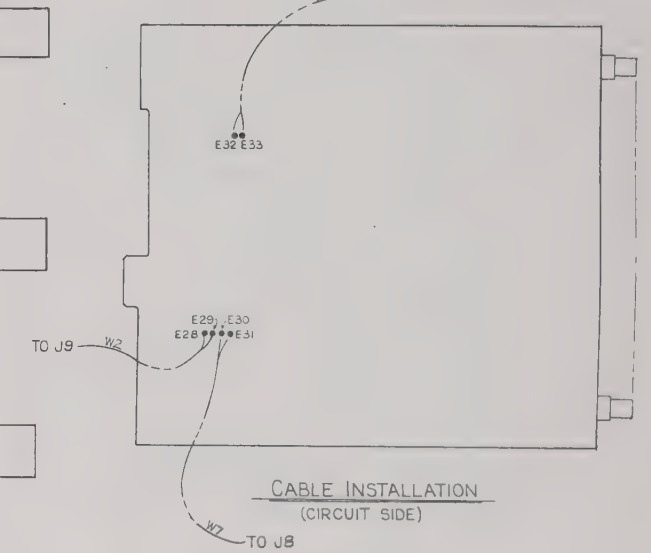
REV	ECN	BY	DATE	APP
E	#4916, C176 ADDED	DT	7/10/85	
F	#4929	DT	7/29/85	A.R.T.
G	#6080	DT	1/9/86	A.R.T.
H	#7644	AT	8/27/86	
J	#7727	JT	10/22/86	J.R.T.

CABLE HOOKUP CHART		
REF DES	DESTINATION FROM	DESTINATION TO
W2	E28	J8 (1100-00-1454)
	E29 ↓	
W7	E30	J9 (1100-00-1454)
	E31 ↓	
W9	E32	J14 (1100-00-1454)
	E33 ↓	
W13	E16	E18
	E17 ↓	E19 ↓
W14	E20	E22
	E21 ↓	E23 ↓
W16	E24	E26
	E25 ↓	E27 ↓
W18	E40	E42
	E41 ↓	E43 ↓
W19	E44	E46
	E45 ↓	E47 ↓





CABLE INSTALLATION
(COMPONENT SIDE)



CABLE INSTALLATION
(CIRCUIT SIDE)

SEE SEPARATE PARTS LIST 1100-00-1455

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 4/23/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PCA, WAVEFORM GENERATOR BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 23	DWG NO 1100-00-1455 REV J
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS NEGTRDER NO A2108

1100-00-1455

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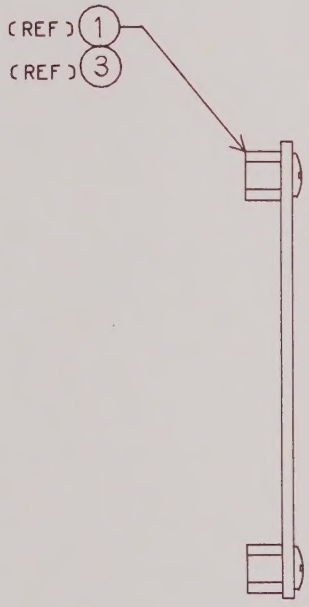
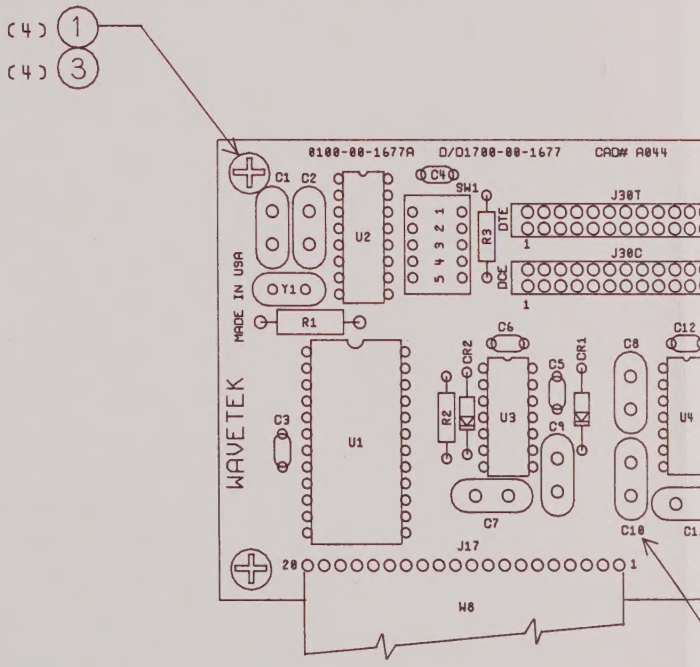


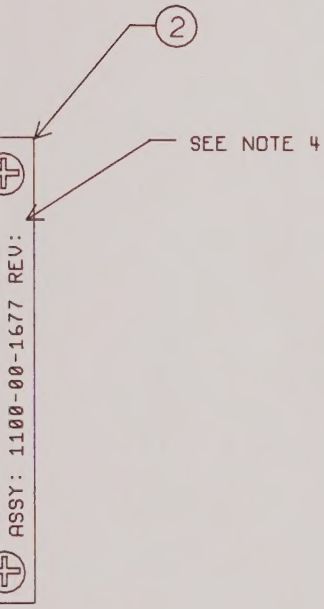


4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC FOR ASSEMBLY INTERCONNECTION.
2. SEE 0103-00-1677 FOR CIRCUIT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION

NOTE: UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

REV	ECN	BY	DATE	APP



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, RS-232 OPTION	0103-00-1677	WVTK	0103-00-1677	1
1	STANDOFF	013-003-2	WVTK	1400-00-2503	4
C12 C3 C4 C5 C6	CAP CER MON 1MF 50V Z5U +80/-20% RAD LD SP .2	SR215E104ZAA	AVX	1500-01-0420	5
C7 C9	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C10 C11 C8	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	3
C1 C2	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	2
2	RS-232 OPTION BOARD	1700-00-1677	WVTK	1700-00-1677	1
J30C J30T	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0136	2
Y1	CRYSTAL, 2.4576 MHZ	VF246	VA-FI	2300-99-0019	1
3	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
R1	RES, C, 1/2W, 5%, 10M	RC-1/2-106J	STKPL	4700-25-1005	1
R2	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R3	RES, MF, 1/8W, 1%, 6.04K	RN55D-6041F	MEPCO	4701-03-6041	1
CR1 CR2	DIODE	1N5282	FAIR	4801-01-5282	2

WAVETEK PARTS LIST	TITLE PCA, RS-232 OPTION	ASSEMBLY NO. 1100-00-1677	REV A
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
SW1	SWITCH PC	500-103	DUNCN	5199-00-0001	1
W8	CABLE, FLEXIBLE FLAT 2", 20 PIN	1-88663-9	AMP	6001-60-0008	1
U3	IC, QUAD LINE DRIVER, RS-232C	MC1488	MOT	8000-14-8800	1
U4	IC, QUAD LINE RECEIVER, RS-232C	MC1489L	MOT	8000-14-8900	1
U1	IC, 1.0 MHZ ASYNCH COMM INTERFACE ADAPTER	MC6850	MOT	8000-68-3000	1
U2	IC, CMOS PROG BIT RATE GENERATOR	HD-4702-9	HARIS	8004-70-2900	1

WAVETEK PARTS LIST	TITLE PCA, RS-232 OPTION	ASSEMBLY NO. 1100-00-1677	REV A
		PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 3/20/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJENGR	8/26/85	TITLE PCA, RS232 OPTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 23/75	DWG NO. 1100-00-1677 REV A
	SCALE 2:1	CODE IDENT 23338	SHEET 1 OF 1

1100-00-1677 A

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